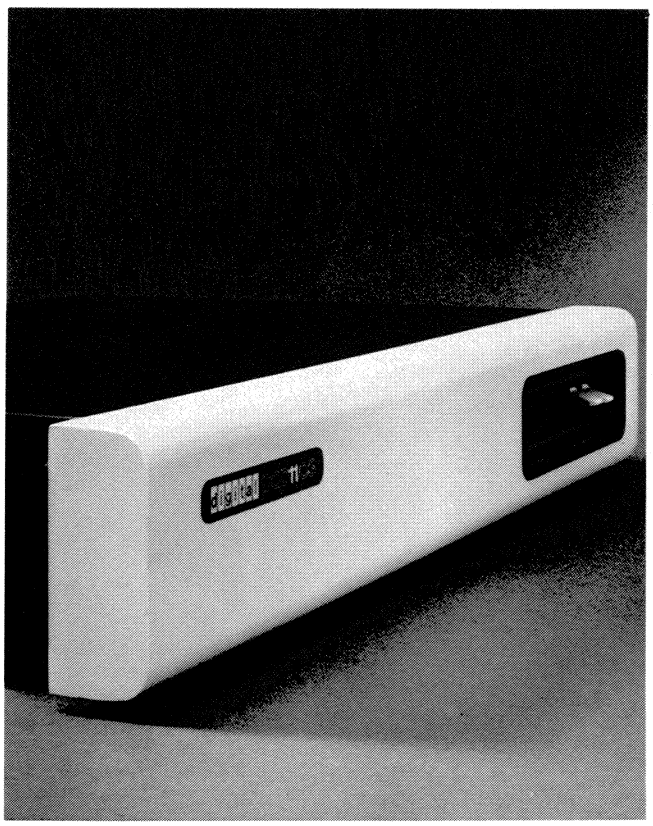
PDP-11

PDP-11/03

digital

JULY 1976

The PDP-11/03 is a complete and powerful mini-computer on four integrated circuit chips. These large-scale-integrated circuits are mounted on a single 8½ by 10½ inch printed circuit board contained within a rack mountable 3½ x 19 x 13½ inch assembly. These chips provide over 400 instructions in an addressing and I/O structure usually found only in much larger and more costly computers. Such features as hardware stack processing, eight general purpose registers, vectored interrupts and single and double operand addressing are standard.



FEATURES:

- Small size (four LSI chips) in a convenient package
- Powerful instruction set
  - over 400 instructions
  - single and double operand addressing
  - 16-bit word and 8-bit byte processing
  - eight general purpose registers
  - hardware stack processing
- Powerful I/O structure
  - vectored interrupts
  - priority structured I/O
  - LSI bus, a subset of the UNIBUS
  - Direct memory access for high speed peripherals
  - asynchronous handling of peripherals
- Choice of solid-state or core memory
- Power-fail/auto-restart
- Real-time clock input

DESCRIPTION

Powerful Instruction Set

More than 400 instructions make up the extensive instruction set. This instruction set (also used by the PDP-11/35,40) permits the user to take advantage of standard PDP-11 software. The only departure from the standard software is the addition of two new instructions, used to explicitly access the processor status word. Development programs, as in the rest of PDP-11 family, include assemblers, linkers, editors, loaders, utility packages, operating systems, and higher level languages.

Extensive Computer Power and Small Processor Size

The processor module is built around a set of four N-channel metal oxide semiconductor (MOS) chips, which include control and data elements as well as two micro-coded read-only memories (microms). The latter are programmed to emulate the powerful PDP-11/34 instruction set, along with routines for on-line debugging techniques (ODT), operator interfacing, and boot-strap loader capability. The processor also contains a 16-bit buffered parallel input/output (I/O) bus, a 4096-word MOS random-access memory (RAM), a real-time clock input, priority interrupt control logic, power-fail/auto restart, and other features to provide stand-alone operation. The entire processor, plus all of the above-mentioned features, are contained on one 8.5-by-10-inch printed circuit board.

Modularity

The processor, memory, device interfaces, backplane, and interconnecting hardware are all modular in design. Module selection, such as the type and size of memory, and device interfaces, enable custom tailoring to meet specific application requirements. The asynchronous, bidirectional LSI-bus structures permit easy expansion of peripherals. In addition, interfaces are less complex, less costly, because addresses and data are multiplexed on the common bus.

Choice of Memory

Memory modules are offered for applications requiring more storage than is available with the 4096-word MOS random-access memory on the processor board. Included are a nonvolatile 4096-word memory, a 4096-word dynamic RAM which can be automatically refreshed either by central processor microcode, or an external refresh circuit, and read-only memory (PROM/ROM) with capacity to a maximum of 4096 words in 512-word increments (2048 words in 256-word increments).

Power-Fail/Auto Restart

Whenever DC power sequencing signals indicate an impending AC power loss, a microcoded power-fail sequence is initiated. When power is restored, the processor can automatically return to the run state. Four options are available for power up sequencing.

Addressing

Much of the power of the processor is derived from its wide range of addressing capabilities. Processor addressing modes include sequential forward or backward addressing, address indexing, indirect addressing, 16-bit word addressing, 8-bit byte addressing, and stack addressing. Variable-length instruction formatting allows a minimum number of words to be used for each addressing mode. The result is efficient use of program storage space.

Peripherals

A full line of peripherals are being added to meet a wide variety of needs. These include the LA36 DECwriter terminal, the LA180 DECprinter, the RX11 floppy disk, and communications interfaces.

Software

Software includes RT-11 real-time disk operating system, multi-user BASIC, single user BASIC, and FORTRAN.

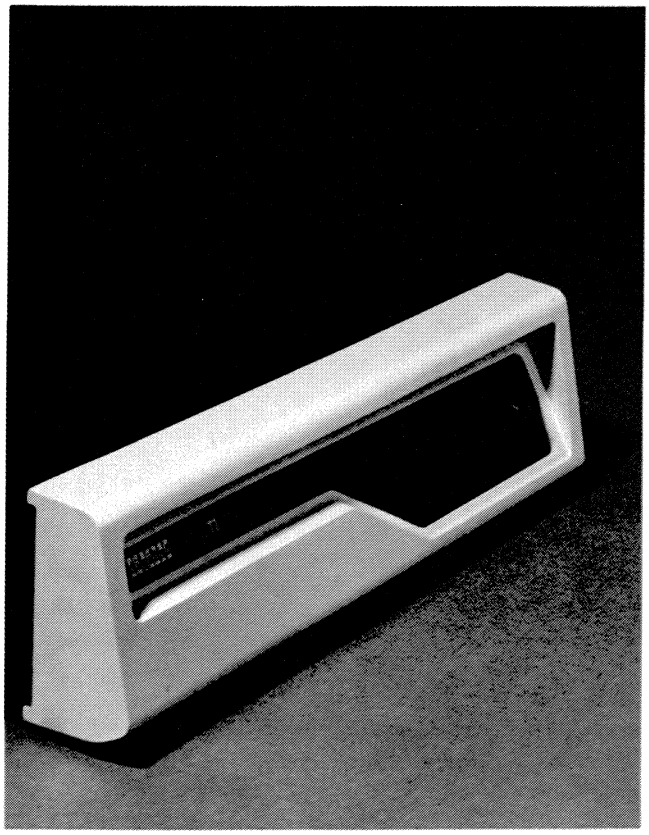
PDP-11

PDP-11/04

JULY 1976

The PDP-11/04 is a low-end member of the PDP-11 family of processors with an excellent performance/price ratio. As a microprogrammed processor, the PDP-11/04 CPU is so compact that the entire CPU logic is contained on one circuit board. This provides greater flexibility during later system expansion by making additional chassis space available.

A number of "large system" features incorporated into the PDP-11/04 CPU as standard options increase its capabilities beyond those found in other computers in its class, and provide considerable flexibility in the use, maintenance, and expandability of any PDP-11/04 based system.



FEATURES:

- Self-test diagnostic routines which are automatically executed every time the processor is powered up, the console emulator routine is initiated, or the bootstrap routine is initiated.
- Operator front panel with built-in CPU console emulator that allows control from any ASCII terminal without the need for the conventional front panel with display lights and switches.
- Automatic bootstrap loader which allows system restart from a variety of peripheral devices without manual switch toggling or key-pad operations.
- Choice of core or MOS memory, with parity memory optional.
- Choice of 5¼ inch or 10½ inch high mounting chassis.

DESCRIPTION

CPU Console Emulator

The "CPU Console Emulator" feature permits control of the PDP-11/04 from any ASCII terminal connected to the processor. Console emulator operations include the normal memory LOAD, EXAMINE and DEPOSIT, in addition to START or BOOT.

Automatic Bootstrap Loader

To simplify program loading whenever the system is "brought up" or reloaded, an automatic bootstrap loader is included with the PDP-11/04 processor.

Automatic Self-Test Feature

To assure the viability and performance readiness of the PDP-11/04 processor, a multi-function CPU test routine has been incorporated into the processor's bootstrap ROM. It is invoked every time upon initiation of the console emulator routine, and when the system is loaded with the automatic bootstrap loader, to guarantee that the basic instruction set, the internal data paths, and the lower 28K words of memory are in operational condition.

Maintenance Feature in Optional Programmer's Console

As another step towards greater reliability and serviceability of PDP-11/04 based systems, the 11/04 includes a maintenance feature which aids in system error diagnosis. When in maintenance mode, the CPU's microcode can be single-stepped, and UNIBUS addresses as well as data can be displayed with the optional programmer's console.

The 11/04 also includes the following big computer features which are part of the PDP-11 architecture.

Powerful instruction set

The comprehensive instruction set and addressing modes (yielding over 400 commands) offer the programming flexibility of a large computer in a 16-bit mainframe. The set provides many extra commands, so that a single instruction frequently suffices where several may be required in a traditional computer. For example, a Bit Test Instruction (BIT) can test any bit or combination of bits to determine their state.

Bit, byte and word addressing in both single- and double-operand formats make memory saving possible and simplify the implementation of control and communications applications.

Instructions make use of the processor's eight general-purpose registers, eight addressing modes, and operate on both words and bytes—making these processors ideal for data communications applications.

Powerful I/O structure

A key factor of the PDP-11 Family's success is that all system elements—processor, memory, peripherals—plug into a single asynchronous high-speed bus, which transfers all addresses and data. Known as the UNIBUS, this bidirectional bus enables easy interfacing and simplifies the construction of multiprocessor or shared peripheral configurations.

The UNIBUS prevents PDP-11 systems from becoming obsolete. Because it is asynchronous, the UNIBUS is compatible with devices that operate over a wide range of speeds. Faster devices or memory can always replace older versions without affecting the system.

Through the UNIBUS, fast devices have easy direct-memory access, requiring no multiplexers or synchronous DMA hardware. These devices can send, receive or exchange data without processor intervention and without intermediate buffering in memory.

The interrupt system for the PDP-11 is another departure in small-computer technology. With fully-vectored interrupts, the system eliminates the high-overhead software that determines the device service routine and code necessary to save system status. The multilevel hardware interrupt system is a standard PDP-11 feature, not an extra-cost option.

PDP-11 minicomputer systems consist of four priority levels, each of which can handle an almost unlimited number of devices. The priority of the device is a function of the device's physical location—the closer to the processor the higher its priority on that level.

The priority system makes excellent use of the PDP-11's hardware stacks. When the processor services an interrupt, it first saves important program information on the stack. This information enables the processor to automatically return to the same point in the program and the same conditions, once the current interrupt(s) has been serviced.

PDP-11
PDP-11/34

digital

JULY 1976

The PDP-11/34 is a midrange member of the PDP-11 family of processors with an excellent performance/price ratio. As a microprogrammed processor, the PDP-11/34 CPU is so compact that the entire CPU logic is contained on two circuit boards. This provides greater flexibility during later system expansion by making additional chassis space available.

A number of "large system" features incorporated into the PDP-11/34 CPU as standard options increase its capabilities beyond those found in other computers in its class, and provide considerable flexibility in the use, maintenance, and expandability of any PDP-11/34 based system.

FEATURES:

- Integral memory management hardware that provides program protection, memory relocation and addressing of up to 124K 16-bit words.
- Integral extended instruction set (EIS) that provides hardware fixed-point arithmetic in double-precision mode (32-bit operands).
- Self-test diagnostic routines which are automatically executed every time the processor is powered up, the console emulator routine is initiated, or the bootstrap routine is initiated.
- Operator front panel with built-in CPU console emulator that allows control from any ASCII terminal without the need for the conventional front panel with display lights and switches.
- Automatic bootstrap loader which allows system restart from a variety of peripheral devices without manual switch toggling of key-pad operations.
- Choice of core or MOS parity memory.
- Choice of 5¼ inch or 10½ inch high mounting chassis

DESCRIPTION

Memory Management and User Protection

The PDP-11/34's integral memory management facility allows a 16-bit machine to provide 18-bit capability for a sizeable extension of addressable memory. Through this facility, system memory can be expanded from its basic 28K words to a maximum of 124K words, more than 4 times its normal memory capacity.

The user has access to this memory in up to 32K units through 8 programmable registers. These registers assign (or map) the user's virtual addresses, in 4K pages, to 4K physical addresses anywhere within core memory. The starting address of each 4K physical segment is stored in the registers.

The user need only provide virtual addresses; transformation to physical addresses takes place automatically and transparently.

Memory management provides two additional features useful especially in a multi-user environment:

1. Memory protection, which can be invoked by designating selected memory segments as "no access" or "read only" areas.
2. Selective swapping, which prevents the unnecessary swapping (out) of memory segments not modified while memory resident, making swapping of user programs more efficient.

CPU Console Emulator

The "CPU Console Emulator" feature permits control of the PDP-11/34 from any ASCII terminal connected to the processor. Console emulator operations include the normal memory LOAD, EXAMINE and DEPOSIT, in addition to START or BOOT.

Automatic Bootstrap Loader

To simplify program loading whenever the system is "brought up" or reloaded, an automatic bootstrap loader is included with the PDP-11/34 processor.

Automatic Self-Test Feature

To assure the viability and performance readiness of the PDP-11/34 processor, a multi-function CPU test routine has been incorporated into the processor's microcode and bootstrap ROM. It is invoked every time the processor initiates a power up sequence, upon initiation of the console emulator routine, and when the system is loaded with the automatic bootstrap loader, to guarantee that the basic instruction set, the internal data paths, and the lower 28K words of memory are in operational condition.

Maintenance Feature in Optional Programmer's Console

As another step towards greater reliability and serviceability of PDP-11/34 based systems, the 11/34 includes a maintenance feature which aids in system error diagnosis. When in maintenance mode, the CPU's microcode can be single-stepped, and UNIBUS addresses as well as data can be displayed with the optional programmer's console.

The 11/34 also includes the following big computer features which are part of the PDP-11 architecture.

Powerful instruction set

The comprehensive instruction set and addressing modes (yielding over 400 commands) offer the programming flexibility of a large computer in a 16-bit mainframe. The set provides many extra commands, so that a single instruction frequently suffices where several may be required in a traditional computer. For example, a Bit Test Instruction (BIT) can test any bit or combination of bits to determine their state.

Bit, byte and word addressing in both single- and double-operand formats make memory saving possible and simplify the implementation of control and communications applications.

Instructions make use of the processor's eight general-purpose registers, eight addressing modes, and operate on both words and bytes—making these processors ideal for data communications applications.

Powerful I/O structure

A key factor of the PDP-11 family's success is that all system elements—processor, memory, peripherals—plug into a single asynchronous high-speed bus, which transfers all addresses and data. Known as the UNIBUS, this bidirectional bus enables easy interfacing and simplifies the construction of multiprocessor or shared peripheral configurations.

The UNIBUS prevents PDP-11 systems from becoming obsolete. Because it is asynchronous, the UNIBUS is compatible with devices that operate over a wide range of speeds. Faster devices or memory can always replace older versions without affecting the system.

Through the UNIBUS, fast devices have easy direct-memory access, requiring no multiplexors of synchronous DMA hardware. These devices can send, receive or exchange data without processor intervention and without intermediate buffering in memory.

The interrupt system for the PDP-11 is another departure in small-computer technology. With fully-vectored interrupts, the system eliminates the high-overhead software that determines the device service routine and code necessary to save system status. The multilevel hardware interrupt system is a standard PDP-11 feature, not an extra-cost option.

PDP-11 minicomputer systems consist of four priority levels, each of which can handle an almost unlimited number of devices. The priority of the device is a function of the device's physical location—the closer to the processor the higher its priority on that level.

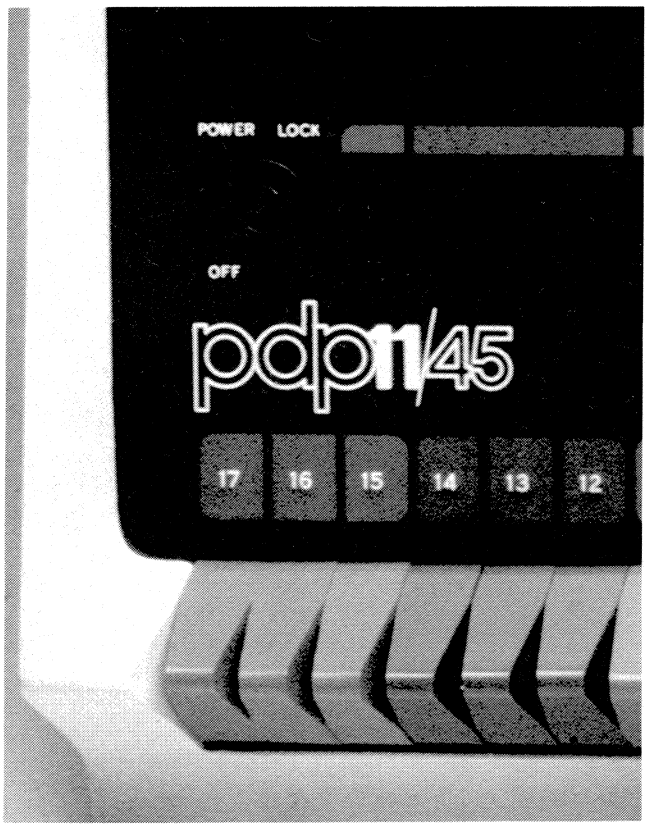
The priority system makes excellent use of the PDP-11's hardware stacks. When the processor services an interrupt, it first saves important program information on the stack. This information enables the processor to automatically return to the same point in the program and the same conditions, once the current interrupt(s) has been serviced.

PDP-11
PDP-11/45

digital

JULY 1976

The PDP-11 is optimized for speed. The extremely high-speed CPU circuits allow program execution speeds in excess of three million instructions per second. The memory systems are just as state-of-the-art. Bipolar memory is available at a speed of 300 nanoseconds. Core memory is available at a speed of 980 nanoseconds. They may be combined on a single system up to a total of 32K bipolar and core to 128K. High speed computations are performed by an independent floating point processor. It overlaps its operations with that of the central processor and offers average double precision multiply times of 5.43 microseconds, working right within its own set of 64-bit accumulators.



FEATURES:

- Memory expandable to 256K bytes.
- Memory segmentation, protection and relocation.
- Option FP11-C floating point processor with advanced features and operation with 32-bit and 64-bit numbers.
- Reliable core memory.
- Fast secondary bus between processor and solid-state memory which operates in parallel with the UNIBUS.

DESCRIPTION

The PDP-11/45 also includes the following big computer features:

Powerful instruction set

The comprehensive instruction set and addressing modes (yielding over 400 commands) offer the programming flexibility of a large computer in a 16-bit mainframe. The set provides many extra commands, so that a single instruction frequently suffices where several may be required in a traditional computer. For example, a Bit Text Instruction (BIT) can test any bit or combination of bits to determine their state.

Bit, byte and word addressing in both single- and double-operand formats make memory saving possible and simplify the implementation of control and communications applications.

Instructions make use of the processor's eight general-purpose registers, eight addressing modes, and operate on both words and bytes—making these processors ideal for data communications applications.

Powerful I/O structure

A key factor of the PDP-11 Family's success is that all system elements—processor, memory, peripherals—plug into a single asynchronous high-speed bus, which transfers all addresses and data. Known as the UNIBUS, this bidirectional bus enables easy interfacing and simplifies the construction of multiprocessor or shared peripheral configurations.

The UNIBUS prevents PDP-11 systems from becoming obsolete. Because it is asynchronous, the UNIBUS is compatible with devices that operate over a wide range of speeds. Faster devices or memory can always replace older versions without affecting the system.

Through the UNIBUS, fast devices have easy direct-memory access, requiring no multiplexers or synchronous DMA hardware. These devices can send, receive or exchange data without processor intervention and without intermediate buffering in memory.

The interrupt system for the PDP-11 is another departure in small-computer technology. With fully-vectored interrupts, the system eliminates the high-overhead software that determines the device service routine and code necessary to save system status. The multi-level hardware interrupt system is a standard PDP-11 feature, not an extra-cost option.

PDP-11 minicomputer systems consist of four priority levels, each of which can handle an almost unlimited number of devices. The priority of the device is a function of the device's physical location—the closer to the processor the higher its priority on that level.

The priority system makes excellent use of the PDP-11's hardware stacks. When the processor services an interrupt, it first saves important program information on the stack. This information enables the processor to automatically return to the same point in the program and the same conditions, once the current interrupt(s) has been serviced.

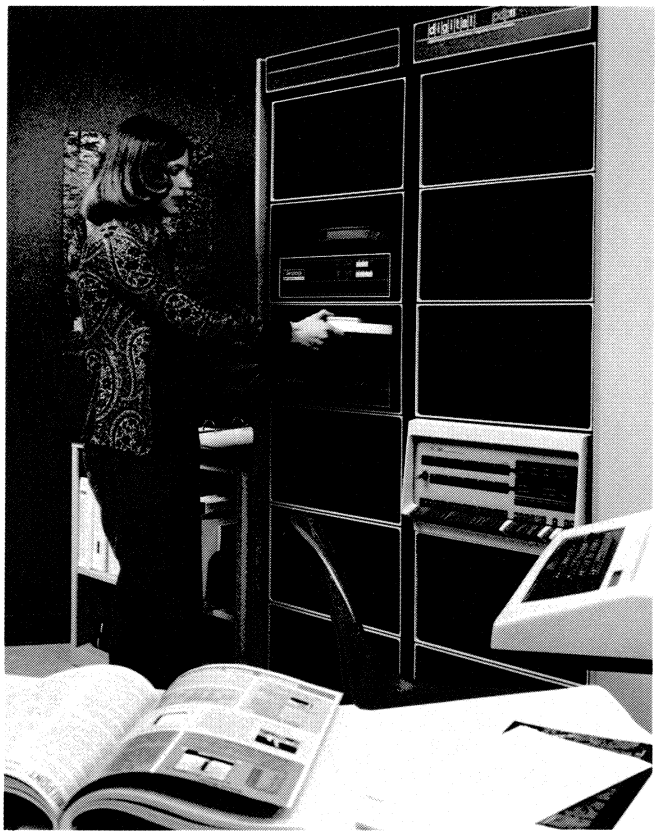
PDP-11

PDP-11/55

digital

JULY 1976

Overlapped operations and high speed components are responsible for the high performance of the 11/55. It takes full advantage of such advanced components as dual ported bipolar memory, a high speed double precision floating point processor, and hardware memory management.



FEATURES

High Speed Components

- 300 nanosecond, dual-ported bipolar memory
- High speed floating point processor with 46 hardwired instructions
- Internal micro-instruction cycle time of 150 nanoseconds
- Instruction execution time of 300 nanoseconds

Overlapped Operations

- Instruction pipelining allows the fetch of the next program instruction to be overlapped with the instruction currently in execution
- Floating point calculation can be performed independent of central processor operations, freeing the CPU to simultaneously perform non-floating point computations.
- Dual bus structure allows direct memory access without cycle stealing on the UNIBUS

Scope

- Up to 256K bytes of combined bipolar and core memory (up to 64K bytes bipolar alone)
- Three CPU operating modes (kernal, supervisor, and user) which enhance system operating efficiency and program protection.
- Hardware memory management, with three sets of memory management registers—one set per CPU operating mode.
- Two sets of eight general purpose registers which, coupled with three CPU operating modes, eliminate the need for saving register contents in a real-time applications environment.
- Direct memory access
- Power fail/auto restart

DESCRIPTION

"LARGE SYSTEM" FEATURES

Extensive Instruction Set

The PDP-11's comprehensive instruction set offers the programming flexibility of a large computer in a 16-bit mainframe. The set provides unusual but often required instructions, so that a single instruction frequently suffices where several may be required in a traditional machine. For example, a bit test instruction (BIT) can test any bit or combination of bits to determine their state. In a conventional machine, this task would require several masking operations.

Bit, byte and word addressing in both single and double operand formats make efficient use of memory and simplify the implementation of control and communications applications.

PDP-11 double operand instructions allow a programmer to perform several operations with a single instruction. For example, ADD A,B adds the contents of location A to location B and stores the result in location B. Three instructions would be necessary with the traditional instruction set:

PDP-11

ADD A,B: Add contents of location A to location B and store results in location B.

Conventional

LDA A: Load contents of location A into accumulator.
ADD B: Add contents of location B into accumulator.
STA B: Store result in location B.

Due to the UNIBUS, the PDP-11 does not require I/O instructions; the same instruction that performs a register-to-register transfer performs a memory-to-device register transfer or a memory-to-memory transfer. In the double operand instruction ADD A,B therefore, A and B can be registers, a register and a memory location, or two memory locations.

The instruction set contains a full set of conditional branches, eliminating excessive use of "jump" instructions. A branch is also included for overflow of a signed integer. Many computers over-economize and eliminate this branch, thereby requiring a 5 to 8 instruction subroutine. All instructions can directly address the 28K word memory space.

General Registers

There is no single accumulator in the PDP-11; instead, there are 8 general registers that can function as accumulators. In addition, they can be used to specify addresses in a variety of ways. Arithmetic operations between general registers is the simplest from a programming standpoint, and the fastest from a timing standpoint. It is advantageous to use them for operating on frequently accessed data. The general registers can be used to:

- Hold data.
- Point to an address that contains data (indirect or deferred addressing).
- Point to an address, which in turn points to an address that then contains data (2 levels of indirect addressing).
- Contain an (indirect) address which, following use for indirect addressing, is automatically incremented to the next higher address.
- Point to one address; then be automatically decremented to point to the next lower address, before being used.
- Hold the offset number for forming an effective address (adding an offset to a base address).

The architecture of the PDP-11 actually allows any memory location to act like an accumulator (or pointer). The general registers are the only ones that are used for automatic incrementing or decrementing and direct offset addressing.

Hardware Interrupts

The interrupt system for the PDP-11 is another feature generally found only in large computer technology. With fully vectored interrupts, the system eliminates the high overhead software that determines which device service routine to use and the code necessary to save system status. In addition, the multi-level hardware interrupt system is a standard PDP-11 feature, not an extra cost option.

The PDP-11 system consists of four priority levels, each of which can handle an almost unlimited number of devices. The sub-priority of the device is a function of the device's physical position—the closer to the processor, the higher its sub-priority on that level.

The device causing an interrupt provides a direct vector to its own service routine, eliminating the slow and tedious operation of polling all devices to see which one interrupted.

The device also provides status information for its own service routine. Thus the programmer has the flexibility of assigning a device to a higher priority and its service routine to another priority without writing special software.

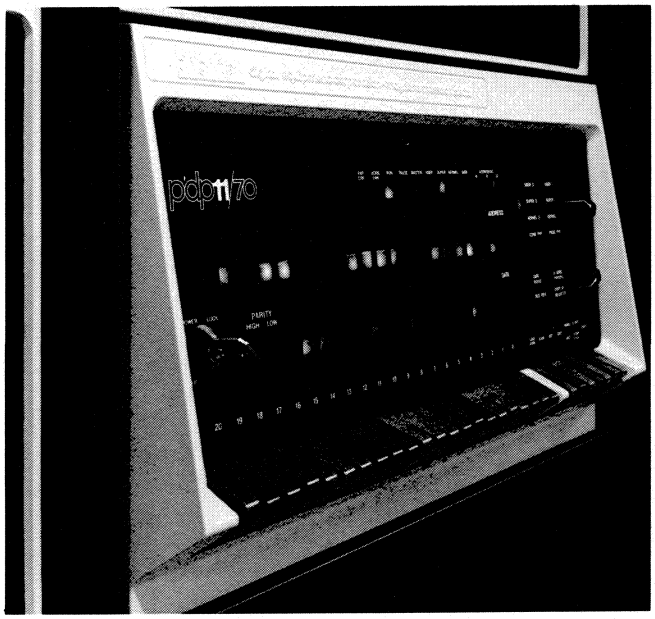
The system also allows interrupts to be enabled or disabled, through software, during program operation. Such masking allows priorities to change dynamically in response to system conditions. For example, a real-time program can disable data entry terminals whenever critical analog data is being collected. As soon as the scan is complete, the terminals can be automatically enabled and ready to input data.

PDP-11
PDP-11/70

digital

JULY 1976

The PDP-11/70 is the most powerful computer in the PDP-11 family. It provides high system throughput in a multi-user, multi-tasking environment requiring large amounts of additional memory; fast response for high performance time-sharing; and computational power for high-speed real-time applications. It is the systems level PDP-11 that combines high throughput with expandability and reliability.



FEATURES

Throughput

- Cache memory organization to provide very fast program execution speed and high system throughput
- 5.8 megabyte I/O bandwidth
- Optional high-speed, mass storage controllers an an integral part of the CPU, to provide dedicated 32-bit paths to high performance storage devices
- Optional high speed floating point processor with 46 hard-wired instructions and operation with 32-bit and 64-bit numbers
- Memory management for relocation and protection in multi-user, multi-task environments
- Fail soft cache memory
- Sophisticated diagnostics

Expandability

- Ability to access up to 4 million bytes of main memory

Reliability

- Extensive parity checking

Compatibility

- UNIBUS for compatibility with the rest of the PDP-11 family

DESCRIPTION

High throughput is comprised of two things– individual component speed and a system organization which efficiently integrates these components. For example, the high speed 11/70 floating-point processor can completely overlap the CPU instruction cycles. The PDP-11/70 is designed for speed, with the power and flexibility to translate processor speed and 32-bit I/O architecture into high system throughput.

Instruction Speed

The PDP-11/70 CPU utilizes high-speed TTL (Schottky) logic pioneered in our PDP-11/45. The circuitry yields a basic execution time of just under 300 nanoseconds. This means, for example, that adding two integers in registers can be performed with one instruction (ADD R0, R1) in just 300 nanoseconds. Internal buffering allows the fetch of the next program instruction to be overlapped with execution of the current instruction.

Cache

An integral cache memory is a standard feature of every PDP-11/70. The cache is a high-speed bipolar memory with a 2,048-byte capacity. It has a cycle time of only 240 nanoseconds. The cache acts like a buffer between the CPU registers and main (core) memory. Whenever a request is made to fetch data from memory, the circuitry checks to see if the data is already in cache. If it is, it is fetched from cache, and no main memory read is required. If not in cache, four bytes are transferred in parallel from main memory for execution. When a request is made to write data into main memory, it is written both into the cache and main memory. This assures that main memory always has the most up-to-date data.

32-Bit Internal Data Paths

To facilitate the transfer of data in and out of the cache memory, the PDP-11/70 utilizes high-speed 32-bit data paths. These internal busses transfer 32 bits (and four parity bits—one per byte) in parallel. Thus, one request can transfer four bytes of data between main memory and cache, or four bytes of data between a high-speed peripheral controller and main memory at direct-memory-access speeds.

Consequently, the high-speed peripheral bus provides up to 5.8 MB/sec band width for high performance peripherals.

Integrated Mass Storage Controllers

The integrated mass bus controllers are high-speed mass storage controllers. They interface devices such as the RP04, RP05 and RP06 disk packs, RS03 and RS04 swapping disks, and the TU16 magnetic tapes to the 32-bit internal data paths. The controllers have been designed to provide high throughput by such features as:

- All controllers can transfer data simultaneously since each controller is connected to the memory system with its own built-in data path.
- While one device on a controller is transferring data, control operations such as seek or rewind may be issued to another device on the same controller. The operation can be initiated and an interrupt generated when it is complete.

Floating-Point Processor

Based on its own set of six 64-bit floating-point accumulators, and 46 additional instructions, the PDP-11/70's floating-point processor carries out high-speed calculations in either single precision (32 bits) or double precision (64 bits).

The basic add, subtract, multiply, divide instructions are complemented by a whole range of additional hardware instructions. Floating-Point Clear, Negate, and Make Absolute instructions allow direct operation on values stored in memory. The Test and Compare instructions allow direct testing for plus, minus, zero, greater than, less than, and equal to. The Convert instructions allow integers (16-bit or 32-bit) to be converted to floating point and loaded into floating accumulators, all in a single operation. These additional instructions allow for faster, more compact coding of computation routines.

Fast as it is, the floating-point processor can give even faster effective computation speeds by taking advantage of overlap. Since the floating-point processor is a separate processor it can operate independently of the central processor. Therefore, during the actual computation time involved in a floating-point operation, the central processor can proceed to execute non-floating instructions. In many cases floating-point execution time is 100 percent overlapped with CPU operation. The overlapped operation also leaves the CPU free to respond to interrupts, so the use of the floating-point unit does not affect the worst-case response to interrupts in real-time applications.
Four factors combine to provide the exceptional computation speed of the PDP-11/70 floating-point processor: fast circuitry, large instruction set, multiple-accumulator architecture, and overlapped operation.

Memory

The PDP-11/70 memory system was designed to meet four criteria. It must provide for very fast data transfer to and from the CPU; it must provide for large capacity and easy expansion; it must provide high reliability and error diagnosis; and it must be cost effective. To provide these functions, the PDP-11/70 memory system utilizes an integral cache memory at 32-bit access for speed, core memory for large-scale capacity, easy expansion, nonvolatility, and cost effectiveness; it also incorporates byte parity and bad block mapping for reliability.
Main memory is composed of core memory modules that are byte addressable and expandable in 64K or 128K-byte increments to a system capacity of just over 4 million bytes. Proven core memory is used to provide maximum price/performance benefits for the system.

Memory Management

The PDP-11/70 memory management unit provides the hardware facilities necessary for complete memory management and protection without any time overhead. It is a memory management facility for accessing all of physical memory and for multi-user, multi-programming systems where memory protection and relocation facilities are necessary.

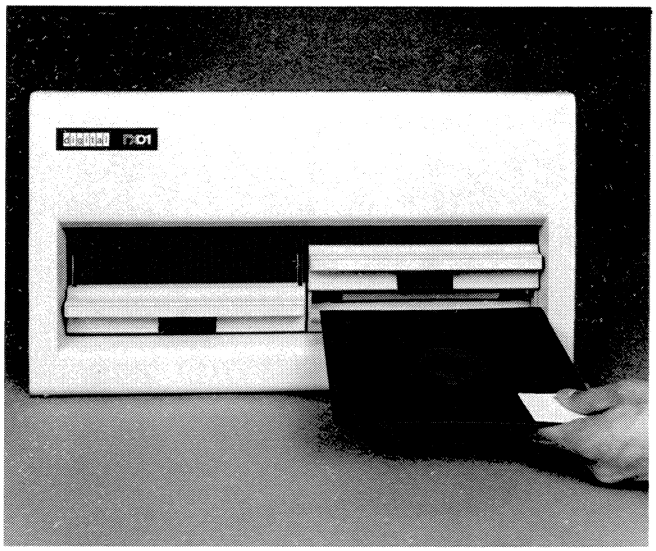
In order to most effectively utilize the power and efficiency of the PDP-11/70 in medium and large scale systems it is necessary to run several programs simultaneously. In such multi-programming environments several user programs would be resident in memory at any given time. The task of the supervisory program would be: to control the execution of the various user programs, manage the allocation of memory and peripheral device resources, and safeguard the integrity of the system as a whole by careful control of each user program.

In a multi-programming system, the memory management unit provides the means for assigning memory pages to a user program and preventing that user from making any unauthorized access to these pages outside his assigned area. Thus, a user can effectively be prevented from accidental or willful destruction of any other user program or the system executive program.

PDP-11
RX11 Floppy Disk System

JULY 1976

The RX11 Floppy Disk System is a highly reliable, low-cost, mass storage subsystem, capable of storing up to 256,256 8-bit bytes per drive in an industry-compatible format. The RX11 provides a compact data interchange and software distribution medium for critical I/O applications. In addition, the RX11's random-access capability allows configuring very low-cost, disk-based systems with small PDP-11 processors. Such systems can satisfy the needs of applications that could never before afford random access storage.



FEATURES

Speed
- 18 microseconds per byte transferred
- 83 milliseconds average latency
- 483 milliseconds average access
- 30 seconds to read the whole diskette

Capacity
- 256K 8-bit bytes/diskette
- 2 drives/controller

Human Engineering
- Extremely simple to load–just insert
- Small and compact–easy to transport or mail
- Preformatted

Reliability
- Simple construction and microprogrammed controller reduce complexity
- Long disk life because head contacts disk only during read/write
- Cyclic redundancy check, longitudinal redundancy check, and parity

Other
- Industry standard preformatting facilitates interchangeability and lowers hardware costs.

DESCRIPTION

The RX11 floppy disk system consists of an RX01 floppy disk drive unit an a PDP-11 quad interface module which requires a single SPC slot. The RX01 includes either one or two drives, a microprogrammed controller module, and a read/write electronics module, all housed in a 10½ inch, rack-mountable chassis. Up to two drives can be supported by each controller for a total storage capacity of 512,512 bytes.

Given an absolute sector address, the RX01 locates the desired sector and performs the indicated function. It automatically verifies head position and generates and verifies the cyclic redundancy check (CRC) character.

Track-to-track moves require ten milliseconds for the move plus twenty milliseconds for settling time if the head is loaded for a read or write. The rotational speed of the diskette is 360 rpm, which results in an average latency time of 83 milliseconds. The track-to-track move, head settling, and latency time produce an average access time of 483 milliseconds. During a sequential access, the whole diskette can be read in about thirty seconds.

The Media

The RX01 floppy disk uses the industry-standard "diskette" or "floppy" media, which are thin, flexible oxide-coated disks similar in size to a 45-rpm phonograph record. The disk is recorded on one side only and is permanently contained in an 8-inch square, flexible envelope.

The envelope has a large center hole for the drive spindle, a small hole for track index sensing, and a large slit for the read/write head. A solenoid contact load pad is located on the opposite side of the envelope. The inside of the envelope is covered with a soft material, designed to wipe the disk surface clean just before reading.

The diskette contains 77 tracks and 26 sectors per track. Each sector can store 128 8-bit bytes for a total formatted capacity of 256,256 8-bit bytes.

The diskette is an ideal storage, interchange, and software distribution medium. Compared to disk cartridges or disk packs, it is very inexpensive. Because it is flat and thin, the diskette is compact, enabling large amounts of data to be conveniently stored in a small space. Diskettes can also be easily transported in a briefcase or in a manila envelope.

The diskette is preformatted in the industry-standard format. However, the file structure is software dependent and may vary from system to system. Preformatted diskettes also reduce hardware costs by eliminating the circuitry required to generate the correct format.

Reliability

The RX01 provides exceptional reliability as well as low cost. The simple mechanical construction of the drive and the use of a microprogrammed controller that reduces hardware complexity contribute to reliability. To enhance disk life, the head contacts the disk only during reading or writing. With the head loaded on a given track, the media can withstand one million passes.

The RX01 performs parity checks and provides error indications. Each sector has a cyclic redundancy check (CRC) character as part of the header field, and another CRC character as part of the data field. The RX01 generates and verifies the CRC characters and provides error indications.

SPECIFICATIONS

Name	RX11
Type	floppy
Formatted Capacity per Drive (bytes)	256K
Number of Drives per Control	2
Formatted Capacity (on-line) per Control (bytes)	512K
Average Access Time	483 ms
Average Transfer Time per Word	36 μsec

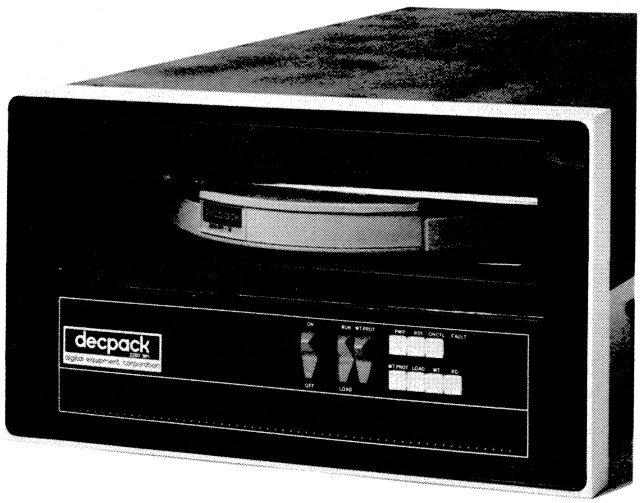
PDP-11
RK05 DECpack

digital

JULY 1976

The RK05 family is DIGITAL's entry level, low cost, disk storage system for PDP-11 computers. The family consists of a controller, a 2.5 MB RK05J disk drive with removable cartridges and a 5MB FK05F non-removable media disk drive. The RK05 family is completely supported by RT11, RSX-11M, RSX-11D, RSTS/E, IAS and MUMPS-11 operating systems.

DIGITAL's rugged and field proven RK05 is the most successful disk product in the minicomputer industry; worldwide, DIGITAL has installed over 20,000 drives.



FEATURES

Speed

- Fast access
- Overlapped seeks for high throughput

Capacity

- 2.5 to 20 million bytes on-line storage per controller
- RK05J with removable cartridges for virtually unlimited off-line storage
- RK05F for economical on-line storage

Human Engineering

- Easy copying from disk to disk
- Easy cartridge handling

Reliability

- Dust protection
- Accurate positioning
- Transfer verification
- Self-contained power supply
- Environment 50°–104° F

DESCRIPTION

The RK05 is a 2.5 megabyte disk drive with removable cartridges. Cartridges recorded on one RK05J can be read on another RK05J and vice-versa. The RK05F is a 5 megabyte non-removable media disk drive. The RK05F is essentially identical to the RK05J except that it has twice the storage capacity, achieved by doubling the track density.

The RK05F has been designed to appear to a controller as if there were two "logical" RK05J drives connected to it. This design feature permits RK05J and RK05F drives to co-exist on the controller for all PDP-11 computer systems. More importantly, the RK05J and RK05F drives are fully compatible in terms of software, diagnostics and programs.

The dual drive disk subsystem consisting of an RK05J and an RK05F with 2.5 MB of removable storage and 5 MB of non-removable storage is an attractive mass storage system. The RK05J, which must always be the first drive on a controller, allows unlimited off-line storage, while the RK05F offers economical on-line storage. Programs and operating systems can be easily loaded on an RK05F or backed up for off-line storage via the RK05J.

Dual drive systems, either RK05J/RK05F or 2 RK05Js, have two independent positioners which allow fast copying of information from one disk to another. In dual drive configurations, the computer system remains operational while removable cartridges are being changed.

The sophisticated controller can overlap seeks on multi-drive systems. While one drive is performing a read or write operation, other drives can be seeking new track locations. Overlapped seeks are currently supported by RSX-11D, RSTS/E and IAS on all RK05J systems but not on mixed RK05J/RK05F systems.

As storage requirements increase, additional capacity can be added via either RK05J or RK05F drives. Existing computer systems which already have a PDP-11 controller (RK11D/RK11C) and an RK05J can be economically upgraded via the RK05F. The RK05F's design eliminates the need for time consuming and extremely expensive program conversions.

The RK05F utilizes two drive positions on a controller instead of the single position utilized by an RK05J. The RK05F is restricted to positions (0,1), (2,3), (4,5), (6,7) on a controller. There must be at least one RK05J drive on a controller and therefore the maximum system configurations (20 MB) for a PDP-11 controller (8 positions) will be 8 RK05J, 2 RK05J/3RK05F, 4 RK05J/2RK05F, etc.

SPECIFICATIONS

	RK05F	RK05J
Capacity	5MB	2.5 MB
Media	Non-removable	Removable cartridge
BPI/TPI	2200/200	2200/100
Data Rate	180 KB/sec	180 KB/sec
Average Latency	20 msec	20 msec
Positioning time		
track-to-track	8.5 msec	10 msec
average	56 msec	50 msec
Dimension	19″x26.5″x10.5″	19″x26.5″x10.5″

PDP-11
RP04/05/06 Disk Pack Subsystem

digital

JULY 1976

The RP04, RP05, and RP06 disk drives are high capacity, high performance disk drives. Each drive, when coupled with a processor-specific controller, becomes a disk subsystem. The feature sheet describes the three drives, and the two subsystems using them.

FEATURES

Speed

- 28 milliseconds average seek
- 1.24 microsecond per byte peak transfer
- Overlapped seeks
- Direct memory access
- Dual access option

Capacity

- 100 million or 200 million 8 bit bytes/disk pack (unformatted)
- 1.6 billion 8 bit bytes/controller maximum

Human Engineering

- On-line pack formatting

Reliability

- Error detection, logging and correction
- Extensive diagnostic software support
- Parity checking on all data and control transfers between controller and disk drive
- Offset positioning

DESCRIPTION

Disk Drive Description

The RP04 and RP05 are 100 million byte disk drives. The RP06 disk drive has double the capacity of the RP04 and RP05, or 200 million bytes. The RP05 is field upgradable to an RP06: the high track density of the RP06 requires different media, read/write circuitry, and heads.

All three drives function identically. Average access time is 36 milliseconds, which includes the time for head positioning and rotational latency. The peak transfer rate is 806,000 bytes per second.

The disk drive is designed for reliability. A phase-lock-loop clock system and modified frequency modulation (MFM) recording offer the latest in reliable reading and recording techniques. Error detection and correction hardware in each drive provides an error correction code (ECC) for correcting any error burst of up to 11 consecutive bits within a 256-byte data field. Software can correct these data field errors without rereading the disk.

Program controlled head offset positioning corrects for slight mechanical misalignment between the heads and the disk pack; the head can be moved about the track centerline in incremental steps. This feature virtually guarantees that packs can be transported between different drives.

To further increase data integrity, the drive has a hardware write-check capability and verification of sector, track, and cylinder positioning. Built-in registers for disk data path checkout simplify maintenance.
Both the RP04 and RP05 use the same disk pack so that packs written on one type of drive can be read on the other. The RP06 uses a newly developed pack which is RP06 specific.

The RP05 and RP06 drives have removable logical address units, which plug into the front of the drive to simplify subsystem reconfiguration.

Disk Subsystem Description

The RP04/05/06 disk drives use the same controllers and can be intermixed.

There are two disk subsystems:

- RP04/05/06 for all UNIBUS PDP-11 systems except the PDP-11/70
- RWP04/05/06 for the PDP-11/70

All subsystems are expandable to eight disk pack drives or 800 million bytes for RP04 and RP05 subsystems, and 1600 million bytes for RP06 subsystems. The removable disk pack offers the flexibility of unlimited off-line storage. All subsystems transfer at the same speed (1.24 microseconds per byte max).

On multi-drive systems, positioning operations can be overlapped for efficiency. While one drive is reading or writing, one or more other drives can be positioning to a new cylinder for the next transfer.

Parity checking is done on both data and control information transfers for increased reliability. The controller also detects and flags memory parity errors. The disk system interrupts the processor on command completion and on error conditions. Extensive error indicators allow on-line diagnostics, and status indicators allow complete program control.

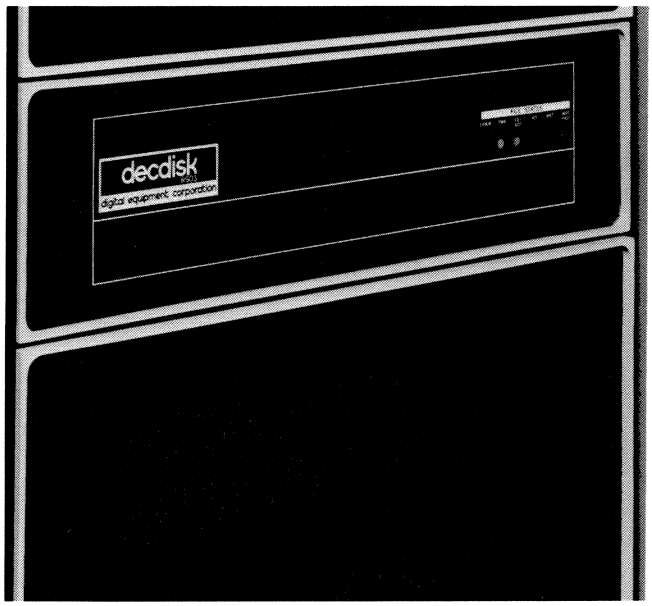
SPECIFICATIONS

Name	RP04	RP05	RP06
Type	pack	pack	pack
Formatted Capacity per Drive (bytes)	88M	88M	176M
Number of Drives per Control	8	8	8
Formatted Capacity (on-line) per Control (bytes)	704M	704M	1408M
Average Access Time	36 msec	36 msec	36 msec
Average Transfer Time per Byte	1.24 usec	1.24 usec	1.24 usec

PDP-11
RS03 and RS04 Fixed Disk System

JULY 1976

The RS03 and RS04 are fixed-head disk systems designed specifically for applications requiring fast, reliable, on-line storage. With an average access time of 8.5 milliseconds and a transfer rate of 4 microseconds per word, the RS03 and RS04 increase throughput substantially for time-sharing applications which involve significant amounts of program swapping. Phase lock loop reading techniques and CRC error detection make these disk systems ideal for real-time data acquisition and control systems requiring a high level of reliability.



FEATURES

Speed

- 2/4 microseconds/word non-interleaved transfer RS04/RS03
- 4/8 microseconds/word interleaved transfer RS04/RS03
- 8.5 milliseconds average access
- Real-time look-ahead
- Overlapped transfer
- Direct memory access

Capacity

- RS03–512K 8-bit bytes/disk
- RS04–1024K 8-bit bytes/disk

Reliability

- Phase lock loop clock system and modified frequency modulation recording
- Write checking
- Prefilter and air filter for clean air
- CRC error detection

DESCRIPTION

The RS03 includes a controller and a rack-mounted RS03 fixed-head disk drive with a storage capacity of 256K 18-bit words. The RS04 includes a controller and a rack-mounted RS04 fixed-head disk drive with a storage capacity of 512K 18-bit words. The RS03 and RS04 are expandable by adding either RS03 or RS04 drives, up to a total of eight drives per controller. A single controller may have a mix of RS03 and RS04 drives. Two drives may be mounted in a single cabinet.

Operation

Data is stored in blocks of 64 words for the RS03 and in blocks of 128 words for the RS04. The RS03 uses one read/write head at a time; the RS04 uses two heads in parallel. There are 64 heads for the RS03 and 128 heads for the RS04. The higher-capacity RS04 records information on both surfaces of the disk, whereas the RS03 uses only one surface. The number of sectors, 64, is the same, but the RS04 achieves double capacity by recording odd-numbered bits on one surface and even-numbered bits on the other surface.

Fast track-switching time permits "spiral" read/write from one track to the adjacent track in a single transfer operation. When the last sector on a track has been transferred, the disk automatically advances to the next track without any delay in the transfer rate. Up to 64K words can be transferred in a single operation.

The RS03 and RS04 also feature real-time look-ahead. This feature permits the program to monitor the current angular position of the disk and thereby minimize access time in a multidrive system when multiple requests are pending. Through the use of interrupts when comparing sectors, program time can be kept to a minimum. Except for the drive currently engaged in a data transfer, all drives can perform searches simultaneously.

Reliability

The RS03 and RS04 offer a high level of data reliability. They have been designed to provide a recoverable error rate of less than 1 in 10^{11} bits read, and a nonrecoverable error rate of less than 1 in 10^{12} bits transferred.

The use of a 16-bit Cyclic Redundancy Check (CRC) character per data block reduces the probability of undetected error to a negligible value. To ensure maximum reliability in the transmission of information between disk drive and control, a differential bus is used with parity generated and checked at the drive and at the control for both control and data transfers.

A phase lock loop clock system and MFM recording offer the latest in reliable reading and recording techniques. In addition, a write-check capability is used to verify data written on any disk without modifying either the disk or the memory data, and without the overhead of a programmed comparison between the original data in memory and the data written on the disk.

SPECIFICATIONS

Name	RS03/RS04
Type	fixed head
Formatted Capacity per Drive (bytes)	512K/1024K
Number of Drives per Control	8
Formatted Capacity (on-line) per Control (bytes)	4M/8M
Average Access Time	8.5 ms
Average Transfer Time per Word	4 or 8/2 or 4

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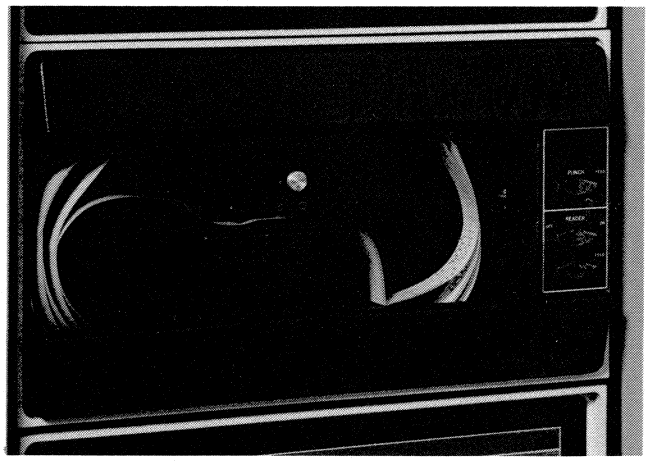
PDP-11

PC11/PR11 PAPER TAPE READER/PUNCH

digital

JULY 1976

The PC11 high speed paper tape reader/punch features automatic fan-fold operation for easier, more reliable handling. It reads eight channel, unoiled perforated paper tape at 300 characters per second and punches at 50 characters per second. A similar system with read only capabilities (PR11) is also available.



FEATURES

Speed

- Read–300 characters/second
- Punch–50 characters/second

Efficiency

- Flexible program control because punch head is independent from the read head
- Automatic fan-fold operation

DESCRIPTION

The tape is read by a set of photodiodes which indicate the presence or absence of holes. The resulting signals are translated into logic levels representing 1's and 0's. Conversely, when punching tape, logic levels representing 1's and 0's are converted into punched-tape format.

Any information read or punched is parallel-transferred through the PC11 control. When an address is placed on the UNIBUS, the control decodes the address and determines if the reader or punch has been selected. If one of the four device register addresses is selected, the control also determines whether an input or an output operation should be performed. An input operation initiates when the processor transmits a command to the paper-tape reader status register. An output operation initiates when the processor transfers a byte to the paper-tape punch buffer register.

Both reader and punch can be operated independently of each other. Either device can be under direct program control (flag check), or they can be operated by interrupts.

The PC11 high-speed paper tape reader/punch control is a set of three modules that form a complete interface for the high-speed reader/punch (PC05) to the PDP-11 UNIBUS. The interface accepts data from the UNIBUS for direct transfer to the HSP data buffer. The interface also provides the gating of the HSR data buffer to the UNIBUS. All data transfers result from programmed commands received from the UNIBUS and are decoded within the interface logic. This logic can also request the UNIBUS and interrupt the processor program so that transfer operations can be performed.

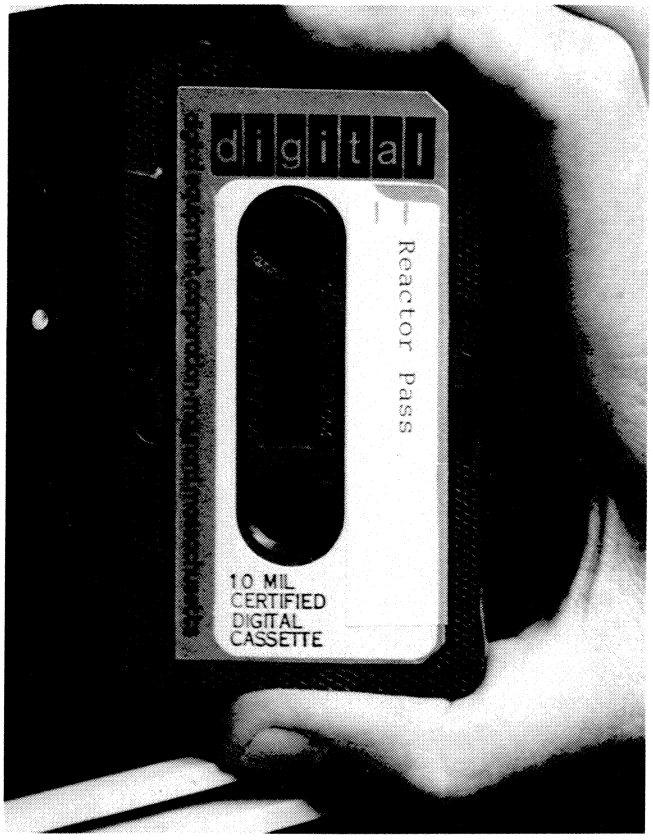
The PR11 high-speed paper tape reader and control is also available for reader-only interfacing to the UNIBUS.

PDP-11

TA11 Magnetic Tape Cassette

JULY 1976

The TA11 magnetic tape cassette system has been designed to provide extremely reliable, trouble-free performance. Features such as low density, wide track recording, heavy mylar tape, phase-encoded recording and cyclic redundancy error checking help eliminate tape failure and ensure accurate data recording and retrieval. At the same time this dual-drive unit is inexpensive enough to replace paper tape.



FEATURES

Speed
- 9.6 inches per second

Capacity
- 92,000 characters

Human Engineering
- Uses magnetic tape cassettes which are easy to insert and remove
- Media is easy to transport and store

Reliability
- 1 MIL TAPE. Heavy mylar backing eliminates edge damage and resultant tape failure.
- REEL-TO-REEL DRIVE. Increases tape life. Only two driving elements. No pinch rollers, capstans, brakes, clutches, pulleys or belts.
- SINGLE TRACK RECORDING. Differentially balanced head eliminates external noise sensitivity. Low density and wide track recording ensure reliability.
- DC MOTORS. Linear servos provide precise, gentle tape acceleration and deceleration, eliminate stretching, and guarantee gap spacing.
- ERROR CHECKING CIRCUITS. 16-bit cyclic redundancy check.
- PHASE-ENCODED RECORDING. Read by sensitive, noise-immune peak detection circuits and phase lock loop.
- SERVICEABLE. Electronics, drives and power supply are easily accessible plug-in subassemblies.
- SOLID-CASTING DRIVE. All elements needed to control tape position, skew and motion are mounted on precision solid casting.
- MODIFIED HUB. Optimizes data capacity, simplifies loading.
- LEADER DETECTION. Optical, foolproof, failsafe.
- CASSETTES INTERCHANGEABLE. Assured by precision construction and frequency-independent read electronics.

DESCRIPTION

Data Organization

In the TA11 Cassette System, data is recorded on tape in a single bit-serial track of data. Since there is no pre-recorded timing or format track (such as in DECtape), data must be sequentially recorded and retrieved as in conventional magnetic tape systems.

The cassette medium is an oxide coated tape with sections of clear leader (no oxide) appended to both ends. Data can not be recorded in these clear leader sections, but they identify BOT (beginning of tape) and EOT (end of tape). Placement of data onto the recordable region of the cassette tape is organized into units called files. Adjacent files are separated by file gaps, which are generated under software control. Each file consists of one or more blocks separated by block gaps. Block gaps are generated automatically. Each block consists of one or more bytes of data and two cyclic redundancy check (CRC) bytes. Under program control, the CRC bytes are appended when a block is written and checked when a block is read. Each byte consists of eight bits (no parity). The number of files, blocks per file, and bytes per block is unrestricted, except for tape capacity. Tape capacity is 92,000 bytes, minimum. This is reduced by 300 bytes per file gap and 46 bytes per block gap.

Controls & Indicators

There are three manual controls on the tape drive. Each drive contains a separate REWIND pushbutton and a Power-On indicator. The Power ON/OFF toggle switch for the entire transport is located on the chassis rear panel. These manual controls and indicators perform the following functions:

Rewind—Pressing this momentary contact pushbutton on one of the two drives rewinds the tape on that drive, at high speed, to the Beginning-of-Tape (BOT) marker provided:

a. a cassette is loaded.

b. tape is not moving under program control.

Pressing this switch during a program controlled operation has no effect.

Power ON/OFF—Placing this switch in the ON position lights both Power-On indicators (located opposite the REWIND pushbuttons on the lower door of each drive) and activates the internal dc power supply. Conversely, placing this switch in the OFF position deactivates the power supply and turns off both Power-On indicators.

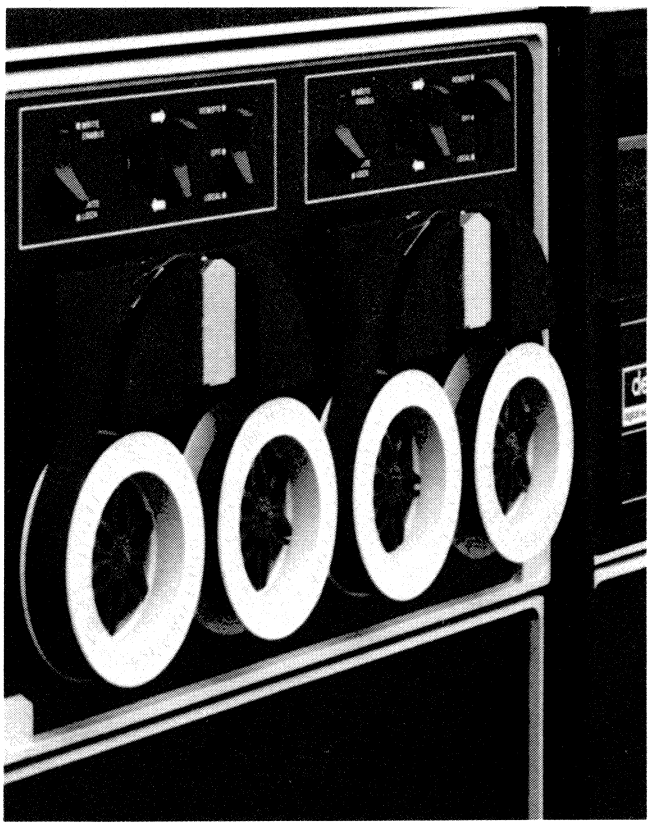
SPECIFICATIONS

Name	TA11
Type	cassette
Formatted Capacity per Reel (characters)	90,000
Number of reels per Transport	2
Number of Transports per Control	1
Formatted Capacity (on-line) per Control (characters)	180K
Average Transfer Time per Character	2 msec

PDP-11
TC11 DECtape System

JULY 1976

The TC11 DECtape system provides random access storage on 4 inch magnetic tape reels which can fit in a pocket. Data transfer speed is enhanced by bidirectional reading and writing of files and direct memory access. DECtape is engineered for high reliability as well as convenience and flexibility, e.g., redundant recording (each byte of data is recorded on two separate tracks) and parity checking on each block.



FEATURES

Speed
- 93 ± 12 inches per second
- All operations are bidirectional
- Direct memory access

Capacity
- 147,968 16 bit words in blocks of 256 words each

Human Engineering
- Small reels can be carried in a pocket
- Easy to mount and dismount

Reliability
- No capstan or pinch roller, therefore longer tape life
- Redundant recording of data
- Parity checking on each block
- Less than 1 transient error in 10^{10} characters
- Insensitive to line voltage or frequency variation
- Tape is extremely tough

DESCRIPTION

Reliability
Low maintenance and high reliability is provided by the simple-designed TU56 transport mechanisms. The drives have no capstan or pinch rollers. Two drive motors control each tape transport. Each transport has a read/write head for information recording and playback on five channels of the tape. Each channel has two nonadjacent tracks with windings connected in series to provide complete redundancy. This redundancy provides exceptionally high reliability (less than one transient error in 10^{10} characters). Reliability is further enhanced by a hardware parity checking feature. This reliability permits use of DECtape without the closely controlled environment usually required for other forms of magnetic tape. Parity checking is performed for each block when read in either direction. Reliability is enhanced by using Mylar tape that is coated on both sides.

Convenience
DECtape is unique—convenient pocket-sized reels are handy to carry and easy to mount and dismount. The reels permit convenient, separate filing and mailing of tape files. Each small 3.9 in. reel holds up to 147,968 16-bit words.

High-Speed Operation

The bidirectional operation of DECtape provides high-speed access to stored program and data files. Reading, writing, searching, and updating may be conducted in either direction. Reading and writing is performed at the rate of 5000 16-bit words per second.

Data is recorded in blocks of 256 16-bit PDP-11 words. Each of 578 blocks is assigned a block number. The block number is recorded at both ends of each block; therefore, a block search may be performed in either direction. During a search operation, the current block number is updated in a control unit register for testing by the PDP-11 processor. This means that little processor overhead is required for search operations. Once the desired block is located, it may be updated "in place" and no recopying of subsequent blocks is required.

TC11 DECtape Control Unit

The TC11 DECtape Control Unit buffers and controls information transfers between the PDP-11 control processor and the selected tape transport (one of eight). The processor controls unit selection, tape motion, direction and number of data transfers. The TC11 accepts and interprets these commands through five registers. These registers are assigned memory addresses and can be read or loaded under program control.

SPECIFICATIONS

Name	TC11
Type	DECtape
Formatted Capacity per Reel (characters)	295,000
Number of Reels per Transport	2
Number of Transports per Control	4
Formatted Capacity (on-line) per Control (characters)	1M
Average Transfer Time per Character	10 μsec

PDP-11

TU10W Magnetic Tape System

JULY 1976

The TU10W is a low cost 9-or 7-track magnetic tape system that uses industry standard 200, 556, or 800-cpi NRZI recording format. From one to eight TU10W transports may be interfaced to a PDP-11 by a control unit. Each transport is mounted in a standard 19-inch cabinet. The TU10W sets a new standard for low cost and high quality for small computers.

FEATURES

Speed

- 45 inches per second

Capacity

- 17 million characters (1024 character blocks) on 7-or 9-track tape

Reliability

- Read after write
- Vertical parity, LRC, CRC
- Long tape life because of vacuum column and servo controlled single capstan
- Write protect ring

DESCRIPTION

High Performance

Transfer rates as high as 36,000 characters per second; 45 ips at 800 bpi. Approximately 3 minutes rewind time for 2400-ft. reel.

Low Cost

Most economical tape system in its performance class.

Industry Compatibility

Compatibility with industry standard provides for efficient transfer of data between the PDP-11 and other computer systems; 7-channel at 200, 556, and 800 bpi; 9-channel at 800 bpi.

Long Tape Life

The TU10W uses vacuum columns and a servo-controlled single capstan to control tape motion. The only contact with the oxide surface is at the magnetic head and a rolling contact on one low-friction, low-inertia bearing. Many other transports use dancer arms and pinch rollers that shorten tape life, cause errors, and require frequent adjustment.

High Reliability

Dual-gap, read-after-write head checks parity, character-by-character. Longitudinal Redundancy Check automatically performed on both 7- and 9-channel units; Cyclic Redundancy Check automatically performed on 9-channel units. Ruggedized construction; shock mounted. Power failure interlocks prevent tape damage or data loss.

High Capacity

10½ inch reel capacity permits up to 2400 feet of tape per transport.

Expandable

Up to 8 transports may be driven by one TMB11 controller in any combination of 7- and 9-channel units. Thumbwheel indicator switch selects logical unit assignments.

SPECIFICATIONS

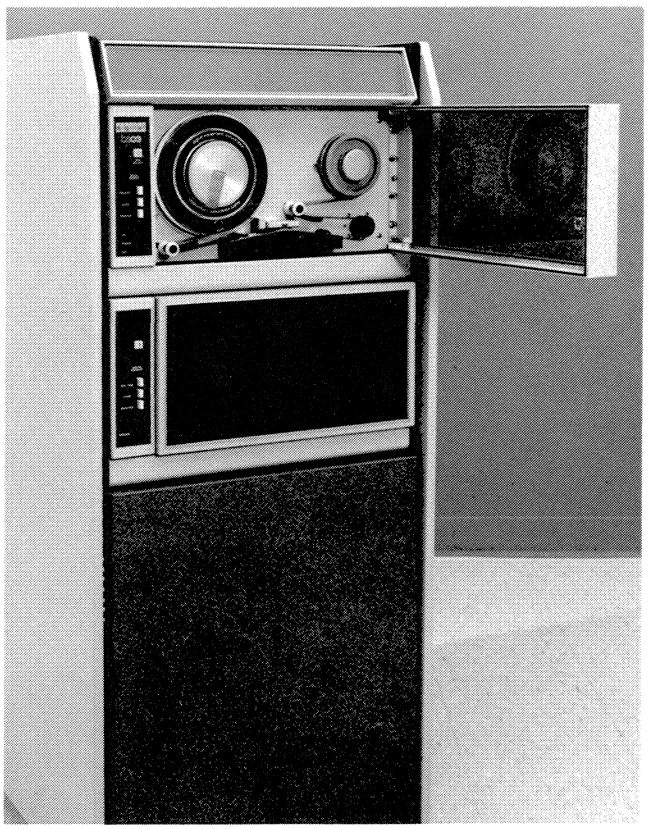
Name	TU10W
Type	magtape
Formatted Capacity per Reel (characters)	20M
Number of Reels per Transport	1
Number of Transports per Control	8
Formatted Capacity (on-line) per Control (characters)	160M
Average Transfer Time per Character	3 μsec

PDP-11
TS03 Magnetic Tape

digital

JULY 1976

The TS03 is a low-cost, 9-track magnetic tape system that uses industry-standard 800-bpi NZRI recording format. The basic system consists of a master tape drive, and a systems unit controller. A second tape drive can be added at the cost of the tape drive only, because the second (slave) drive uses the master drive's controller.



FEATURES

Speed
- 12½ inches per second

Capacity
- 7 inch reels
- 4 million characters (1024 byte blocks) per 9-track tape

Human Engineering
- Small size
- Quiet because no cooling fans are needed

Reliability
- Read after write to eliminate writing hard errors.
- Uses vertical parity, CRC, and LRC error detection codes.
- Linear drive reel serves to prolong tape life.

Other
- Low power consumption

DESCRIPTION

The major features of the TS03 are high reliability, low cost, small size, and low power consumption. The major benefit is that, despite its low cost, the TS03 does not sacrifice reliability. It uses the same techniques to record data in the same manner as larger, more expensive transports, but it does this with a slower, extremely simple mechanism.

Cost savings result from small size because the TS03 frequently fits into existing cabinets. The TS03 occupies 10½" of rack space and can fit into a processor cabinet with spare room left over for another subsystem. The controller occupies a systems unit in the processor expander box.

Small size also means lower power consumption because:
- There is no vacuum motor.
- The TS03 uses very low standby power—about the same as a medium-sized light bulb.
- It takes less power to drive the TS03's seven-inch diameter reels.
- Lower power consumption means a smaller load if back-up generator or batteries are used.
- Heat dissipation is so low that no cooling fans are needed.

The absence of cooling fans also means that the TS03 is quiet—so quiet it cannot be heard running.

Reliability

The TS03 is designed to read and write data to industry standards with high reliability. The calculated MTBF (Mean Time Between Failures) is 5,080 hours for the tape drive.

A unique feature of the TS03 eliminates the writing of hard errors on tape. If an error is detected in the read-after-write check, programming can cause the entire record to be rewritten. Hardware within the TS03 automatically senses that this is a retry and the read-checking margins are tightened up to ensure distinguishing between a transient error and a bad tape area. If the data passes on a second (or subsequent) pass, the written data is guaranteed to exceed the read thresholds. If there was a bad section of tape, the faulty record can be erased, then recorded correctly further down the tape.

SPECIFICATIONS

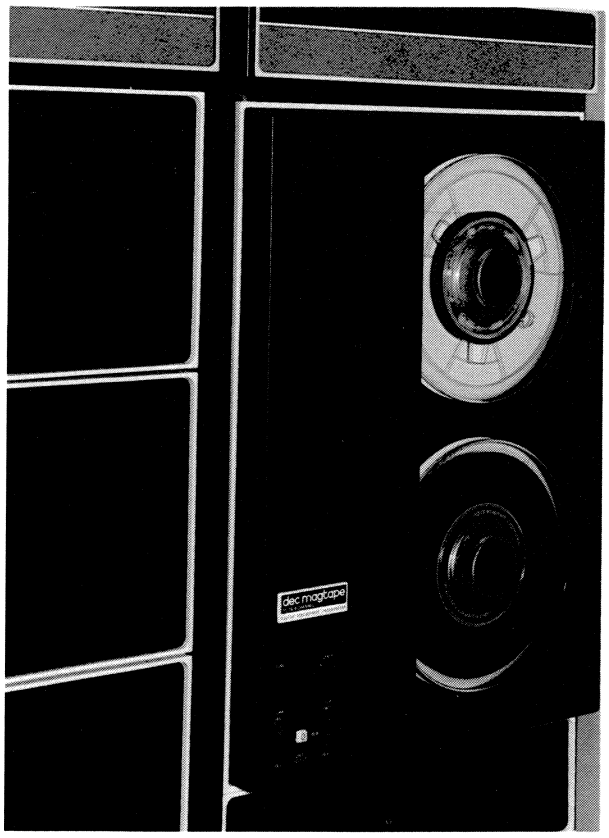
Name	TS03
Type	magtape
Formatted Capacity per Reel (characters)	5M
Number of Reels per Transport	1
Number of Transports per Control	2
Formatted Capacity (on-line) per Control (characters)	10M
Average Transfer Time per Character	10 μsec

PDP-11
TU16 Magnetic Tape Systems

digital

JULY 1976

The TU16 is a highly reliable 9-track tape storage system that uses industry compatible recording formats, with densities of 1600 and 800 bits per inch, selectable under control. Reading and writing are performed at 45 inches/second. Since the industry compatible format is used, data may be easily transferred between computers.



FEATURES

Speed

- 45 inches per second
- Reading in reverse

Capacity

- 26 million bytes (1024 byte blocks) per 9-track tape
- 1–8 drives per controller

Reliability

- Phase encoded on-the-fly error correction
- Read after write
- On-line error and status reporting to CPU.
- Hardware diagnostic capability for off-line diagnostics and test.
- Long tape life because of vacuum column and servo controlled single capstan.
- Parity, LRC, CRC.
- Self clocking not dependent on precise skew control.
- Write protect ring.
- Runaway timer which stops tape if no read or write within a distance of 25 feet.
- Must be at least 12 characters in a block to be recognized as data

DESCRIPTION

Reading can be performed while tape is moving in the forward or reverse direction, but writing occurs only in forward.

Tape motion is controlled by vacuum columns and a servo-controlled single capstan. Long tape life is possible because the only contact with the oxide surface is at the magnetic head and at a rolling contact on one low-friction, low-inertia bearing. The half-inch mylar-base tape is coated on one side with an iron oxide composition. The load and end points of the tape are marked by reflective strips which are detected by photo diodes. Approximately 10 feet of blank tape are wound on a reel, preceding the beginning of tape (BOT) and end of tape (EOT) strips. A gap of about three inches is left from the load point before writing can begin, with NRZI. With PE, an identification burst (IDB) is written in this gap.

There is a provision to prevent accidental writing on a particular tape reel. An industry-standard write-protect ring on the reel is sensed by the tape drive.

Parity is checked character-by-character when reading and writing on tape to verify the accuracy of data transfer. With NRZI, there is also a cyclic redundancy check (CRC) character generated or checked at the end of each record, plus a longitudinal parity check (LPC) character. If an error is detected, an error indication is made.

Reliability

Data reliability of the TU16 tape system is enhanced by the 1600-bpi, phase-encoding, self-clocking feature which is not dependent on precise tape skew control. In addition, the 800-bpi NRZI mode includes a tight read-after-write check. The written data is checked to insure that it far surpasses the minimum allowable reading level.

Bad tape error problems are minimized by a "runaway timer" which allows the system to recover from bad tape sections on the reel. If no reading or writing is performed within a tape distance of approximately 25 feet, tape movement will stop and an error will be indicated. Data will not be acknowledged as comprising a data block unless there are at least 12 characters in the block.

Upgrading

An NRZI 800-bpi-only tape system can be upgraded to have the 1600-bpi phase-encoded capability. An upgrade option is available for installation by DIGITAL Field Service at the customer's site.

SPECIFICATIONS

Name	TU16
Type	magtape
Formatted Capacity per Reel (characters)	32M
Number of Reels per Transport	1
Number of Transports per Control	8
Formatted Capacity (on-line) per Control (characters)	250M
Average Transfer Time per Character	1.4 μsec

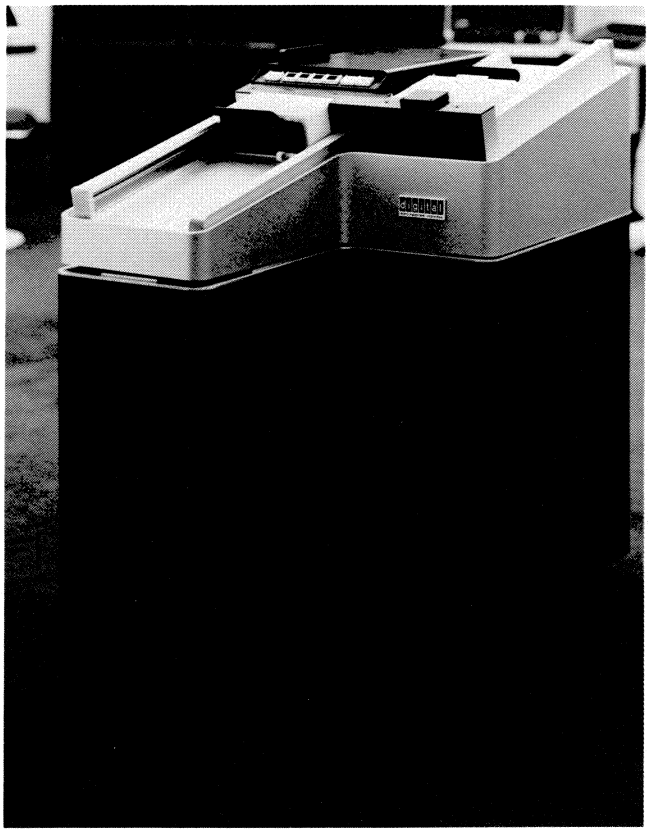
PDP-11
Photoelectric Card Readers

JULY 1976

The photoelectric card readers for the PDP-11 are designed to meet varying throughput requirements and data formats. All readers use the industry standard EIA card that has 80 columns and 12 zones (or rows). The CR11 and CM11 can process punched cards at 285 cards/minute, while the CD11 can process cards at up to 1200 cards/minute.

The CM11 can read cards marked with ordinary pencil or pen; it can also read a mixture of punched hole and mark sense within the same batch of cards or even within the same card.

The CD11 has two versions: a tabletop unit with an input hopper capacity of 1000 cards that operates at 1000 cards/minute; and a free-standing floor model with a large 2250-card hopper that has a speed of 1200 cards/minute.



FEATURES

Speed

- CR11 and CM11–285 cards/minute.
- CD11 table–1000 cards/minute.
- CD11 floor–1200 cards/minute.
- All models achieve higher throughput through a continuous operation feature, i.e., cards may be loaded and unloaded during operation.
- The CD11 transfers data through direct memory access.

Capacity

- CR11 and CM11–400 cards
- CD11 table–1000 cards
- CD11 floor–2250 cards

Human Engineering

- Quiet because of automatic shutdown switch.

Reliability

- Fewer card jams because
  - –higher tolerances
  - –riffle air feed
  - –vacuum picker
  - –short card path
  - –six attempts to read card before rejecting it

Flexibility

- Data formats selectable under program control

DESCRIPTION

Reader design helps prevent card jams and keeps card wear to a minimum. Readers also have a high tolerance to cards that have been nicked, warped, bent or subjected to high humidity.

To keep cards from sticking together, the readers use a special "riffle air" feature. The bottom half inch of cards in the input hopper is subjected to a stream of air which separates the cards and air cushions them from the deck and from each other.

Cards entering the reader are selected through a vacuum picker. The picker and its associated throat block prevent the unit from accepting cards that have been stapled or taped together (unless such taping is on the leading edge). Because the card track is very short, only one card is in motion at any time. This minimizes the chances of cards jamming. Stoppages are also reduced since the reader automatically makes six attempts to process a card before rejecting it.

The read station uses infrared light-emitting diodes (LEDs) as its light source and phototransistors as its sensors. No adjustments are required during the ten-year life expectancy of the diodes.

Because card reader operation is flexible, cards can be loaded and unloaded while the reader is operating. A switch may be set to provide system blower shutdown or continual running after the last card has been read. Automatic shutdown reduces computer room noise level, and indicates that the card hopper is empty.

A control unit is included with the card reader.

Data Formats

The readers are designed to look, sequentially, for data in 80 columns, starting with column number 1. Each column has 12 zones, or rows. A hole (or a mark) is interpreted as a binary ONE, and the absence of a hole (or no mark) as a binary ZERO. Data is read from the card one column at a time. There are two data formats for input to the computer.

Non-Compressed Mode–A separate bit in the data register is used to record the state of each card zone. The 12-zone bits correspond to 12 bits in the PDP-11 word (which has 16 bits).

Compressed Mode–The 12-zone bits are encoded into 8 bits, to fit in a PDP-11 byte (8 bits). More efficient data storage is achieved in this mode. All present Hollerith codes (the standard used for 12-zone card data), and the proposed expansion of the code can be accommodated with the compressed format utilized.

SPECIFICATIONS

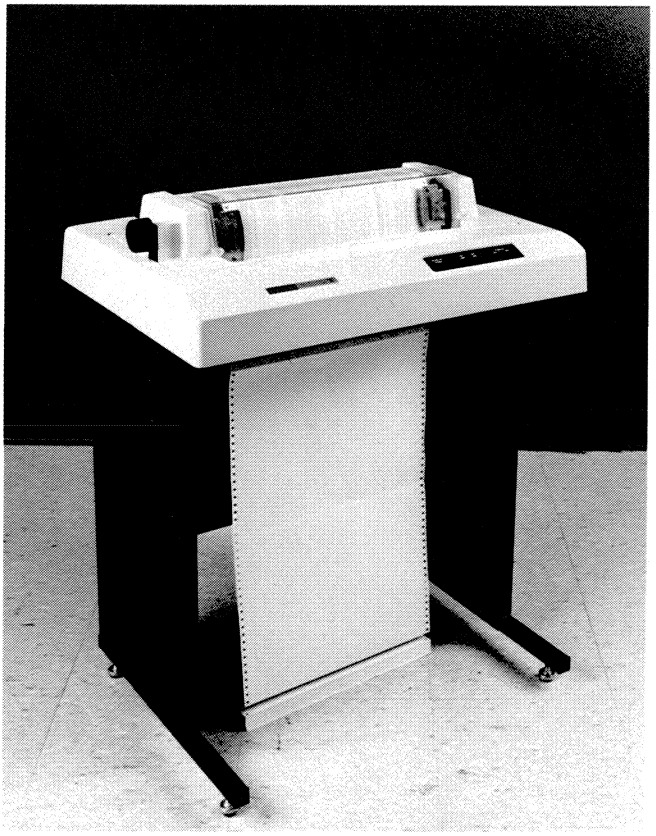
CARD READERS	TYPE CARD	PHYSICAL SIZE	HOPPER SIZE	MAXIMUM CARDS/ MINUTE
CR11	punch	tabletop	550	285
CM11	mark or punch	tabletop	550	285
CD11	punch	free-standing	2250	1200

PDP-11
LA180 Printer

JULY 1976

The LA180 DECprinter I is an inexpensive 7X7 dot matrix 132 column printer that prints at 180 characters per second. It features the 128 character ASCII upper-lower case print set, an extensive array of human engineering features, and may be used either locally or as a remote printer.

The DECprinter I extends the field-proven technology of the LA36 DECwriter II into applications demanding higher speed capabilities.



FEATURES

Speed
- 180 characters/second

Capacity
- 1-6 part forms
- 128 character ASCII upper/lower case print set
- 132 columns

Human Engineering
- Quiet operation because scanning is servo controlled
- Paper out switch
- Forms switch to set top of form and length
- Variable forms width
- Infinitely variable forms adjustment
- Excellent character readability
- Backspace capability
- Ability to compress 132 columns into an 8-inch space to allow printing on 8½ x 11 inch sheets.

Reliability
- Servo controlled scanning for accurate, reliable dot placement

DESCRIPTION

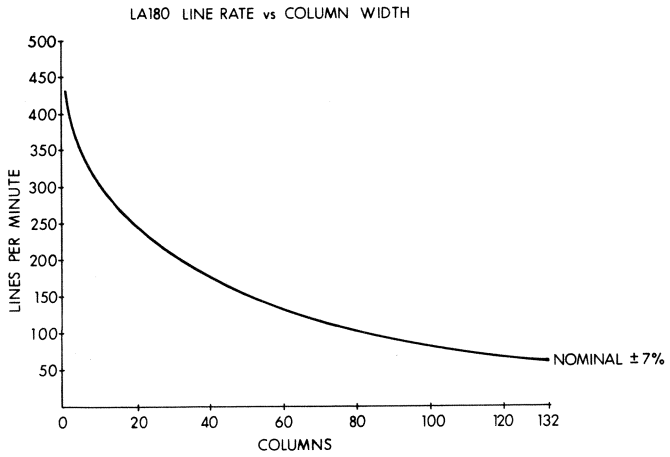
DECprinter I has many operator features which enhance its ease of use. Included are a forms-length switch which sets the top-of-form to any of 11 common lengths, paper-out switch and alarm, and high reliability print-head. Also featured are quiet operation, infinitely variable forms adjustment, variable forms width, and multipart forms capability.

Operation
Seven solenoid-driven wires form the characters by scanning the page from left to right. The scanning motion is servo controlled, thereby assuring accurate dot placement and quiet, reliable operation. The machine prints a line at a time and automatically performs a carriage return upon receipt of a CR, LF, or FF command.

Power-Up
Upon power-up, the DECprinter I is initialized to execute incoming data. The head moves to the left and stops at column 1.

Carriage System
The carriage system transports the head along the horizontal axis of the machine, provides accurate horizontal positioning for character placement, provides printhead adjustment for clean impressions on a variety of forms.

The carriage is controlled by a servo system which assures accurate dot placement. The servo operates in the forward direction at 18 inches per second and has a carriage return time of less than 275 ms.



Ribbon Feed System

The ribbon feed system is driven by the carriage motion only when the carriage is moving from left to right. This prevents ribbon smudging when the DECprinter is not printing.

Paper Feed System

The paper feed system is a stepping-motor-driven tractor feed. The tractor design provides 3-to-4-pin engagement of the form and a flat bed for control and positive feeding of multipart form. Paper may be fine-positioned vertically by pushing the line feed knob inward and rotating it in the direction desired.

SPECIFICATIONS

Name	LA180
Type of Printer	impact
Print Set Number of Characters	128
Maximum Speed in Lines/Minute	60-400
Maximum Column Width	132
Paper Type	standard

PDP-11
LV11 Electrostatic Printer/Plotter

JULY 1976

The LV11 electrostatic printer/plotter provides quiet, reliable printing and plotting at high speeds.

The entire ASCII character set can be printed across 132-column lines at a rate of 500 lines per minute. In plotting mode, the LV11 prints 122,880 dots per second (independent of picture complexity) with a resolution of 1024 dots per line,

FEATURES

- Quiet operation
- Print speeds of 500 lpm
- Plotting speed of 122,880 dots per second with a resolution of 1024 dots per line
- Reliable operation because of few moving parts

DESCRIPTION

The controller (included with the LV11) permits both printing and plotting, and accommodates most DIGITAL line-printer software.

The electrostatic printing technique employs a fixed writing head with 1024 addressable writing electrodes. As the paper passes over the writing head, any, or all, of the electrodes may pass an electric charge through the paper. The charged paper then passes over a liquid toner containing carbon particles. The particles are attracted to the charged areas on the paper, causing the appearance of black dots.

The only moving parts in the LV11 are the paper-moving motor and small toner pump–simplicity of design guarantees long, trouble-free operation.

SPECIFICATIONS

Name	**LV11**
Type of printer	electrostatic
Print Set Number of Characters	96
Maximum Speed in Lines/Minute	500
Maximum Column Width	132
Paper Type	electrostatic

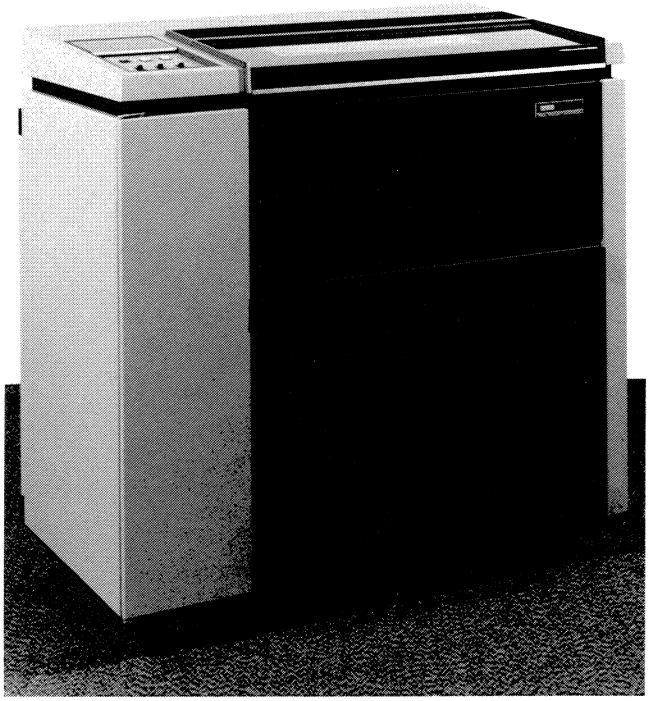
770526

PDP-11
LP11-R AND LP11-S LINE PRINTERS

digital

JULY 1976

The LP11-R and LP11-S are fast reliable drum printers which are designed to handle extremely heavy production loads. The LP11-R has 64 characters and a print speed of 1200 lines/minute. The LP11-S has 96 characters and a print speed of 925 lines/minute. Both have a 132-column line.



FEATURES

Speed
- LP11-R–1200 lines/minute
- LP11-S–925 lines/minute

Capacity
- LP11-R–64 characters
- LP11-S–96 characters
- 132 columns
- 1-6 part forms

Human Engineering
- Rapid paper and ribbon loading
- Vernier adjustment for both horizontal and vertical paper tension

Reliability
- Minimum variability in print line
- Simple rugged hammer mechanism

Other
- Full line buffering

DESCRIPTION

The LP11-R and S require minimum maintenance due to their modular design and integrated circuitry. Paper is loaded by opening the drum gate and placing the paper directly on the tractors. The wide swing of the gate provides complete access to the paper loading area and the print ribbon.

Operator Controls

The operator's control panel, externally located on top of the cabinet, contains the following switches and indicators.

Indicators:

Power–Illuminated when power is on.
Ready–Illuminated when power is on and all interlocks are closed.
On Line–Illuminated when printer is in the ready condition, the print inhibit switch is off, and the on line switch has been actuated.
Drum Gate–Indicates the drum gate is unlatched.
Print Inhibit–Indicates the print inhibit switch is on–hammer fault.
Paper Fault–Indicates the paper is torn or out: ribbon counter alarm or runaway is detected.
Test Mode–Indicates that the printer is running in test mode.

Switches

Test Mode–A momentary switch used for off-line printing. This switch utilizes the decode switches on the test panel.

Top of Form–A momentary switch used to advance the tractors to a top of form position, i.e., channel zero of the tape reader. This switch is disabled when the printer is on line.

On Line/Off Line–A momentary switch that puts the printer on-line and illuminates the on-line indicator. In order to put the printer on-line, the ready indicator must be on and the print inhibit switch must be off. If the printer is on-line and the switch is actuated, the printer will go off-line and extinguish the on-line indicator indicator.

Master Clear–A momentary switch that initializes the printer control electronics.

Main Power–A circuit breaker which allows the operator to enable or disable primary power to the printer.

SPECIFICATIONS

Name	**LP11-R/S**
Type of Printer	impact
Print Set Number of Characters	64/96
Maximum Speed in Lines/Minute	1200/900
Maximum Column Width	132
Paper Type	standard
Number of Copies	6

770526

PDP-11

LP11-V and LP11-W LINE PRINTERS

digital

JULY 1976

The LP11-V and LP11-W 132 column printers are high quality, low-cost drum printers with 64 or 96 characters. They include many user oriented features. For example: a top-of-form control, self-test capability, a switch to accommodate variable-length forms (11 positions, 3 to 14 inches), a static eliminator and a paper receptacle. Forms with up to six parts may be used.

FEATURES

Speed

- LP11-V–300 lines/minute
- LP11-W–230 lines/minute

Capacity

- LP11-V–64 characters
- LP11-W–96 characters
- 132 columns
- 1-6 part forms

Human Engineering

- Variable forms control with top of form
- Paper receptacle
- Vernier for both horizontal and vertical forms adjustment

Reliability

- Static eliminator
- Self-test capability

Other

- Program compatible with other LP11 series printers
- Full line buffering

DESCRIPTION

Operation

Paper and inked ribbon pass between a row of hammers and a continuously-rotating metal drum. The drum surface contains 132 columns of all print characters. Data to be printed is received and stored in a full line buffer. Printing starts when a control character (line feed, carriage return, or form feed) is sent. If more than 132 characters are sent before the control character, the extra characters are disregarded.

Printing is accomplished by scanning the stored characters in synchronization with the rotating drum characters and actuating the appropriate hammer as the desired characters move into the printing position. A 132-column line is printed in two drum revolutions; the odd-numbered columns in one revolution and the even-numbered columns in the second revolution.

Programming

The LP11-V and LP11-W are program-compatible with previous LP11-series line printers. Within the control unit there are two registers, one for printer status, the other to hold the 7-bit ASCII-coded character to be printed. The same register addresses and bit definitions are used.

SPECIFICATIONS

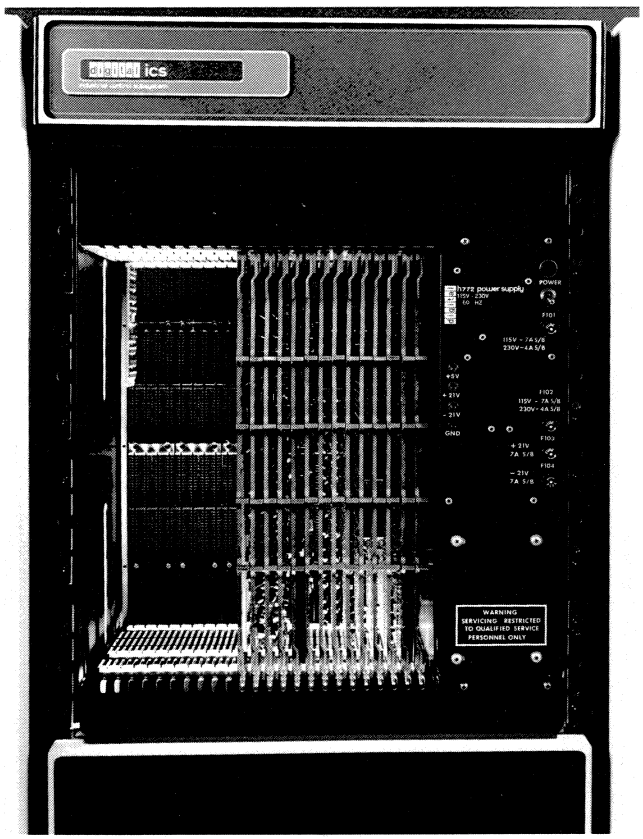
Name	**LP11-V/W**
Type of Printer	impact
Print Set Number of Characters	64/96
Maximum Speed in Lines/Minute	300/230
Maximum Column Width	132
Paper Type	standard
Number of Copies	6

PDP-11
ICS/ICR

digital

JULY 1976

DIGITAL's Industrial Control Subsystem (ICS) is a local process I/O subsystem for interfacing plant signals, actuators, and sensors to PDP-11s. The Industrial Control Subsystem Remote (ICR) is a remote version of the ICS which is connected by a single coax cable to a PDP-11 physically located up to 6,000 feet away.



FEATURES

Power

- Full complement of functional I/O capabilities including AC and DC sense and interrupt, AC and DC output, counters, analog to digital converters, and digital to analog converters.
- Full support of both local and remote subsystems by DIGITAL's advanced family of real-time operating systems: RSX-11D, RSX-11M, and RSX-11S.
- Interfacing of up to 12 ICS/ICR subsystems to a single PDP-11 family computer.

Efficiency

- Implementation of local and remote subsystems utilizing identical functional I/O modules.
- Identical programming of local and remote I/O subsystems.
- Reduced CPU loading and overhead accomplished by automatic hardware polling of remote I/O subsystems.
- Remoting of I/O subsystems at distances up to 6,000 feet from the CPU.
- Status of all remote I/O signals available to the CPU without dialog between the remote I/O subsystem and the CPU.

Reliability

- CPU notification on power loss or restart of remote subsystem.
- Transformer isolation of the coax cable at both the CPU and remote subsystem for increased system integrity.

Ease of Use

- Complete implementation of the Instrument Society of America (ISA) standards for software support of both local and remote I/O subsystems.
- Microprogrammed controller for implementation of all communication functions.
- Industry standard terminal interface (20 milliamp) included on remote subsystem for use in controlling diagnostics, calibration software, and low duty cycle data entry and logging. Hardware error detection and correction without loss of data or CPU intervention.

DESCRIPTION

The ICS/ICR operates under program control as an input/output device capable of interrogating both digital and analog inputs, and driving both digital and analog outputs. One ICS/ICR can handle up to 256 I/O points and a total of 12 ICS/ICR subsystems can be interfaced to a single computer. Any mixture of ICS and ICR subsystems is possible.

The ICR brings the computer interface hardware closer to the source of field signals, thereby reducing field wiring expense. Field signals are digitized and transmitted serially over a single cable connecting the ICR to the PDP-11. The ICR includes hardware implementation of the communication protocols for error detection and recovery without computer intervention or assistance.

From the user's standpoint, the remote subsystem operates identically to the local subsystem. This similarity means programs are compatible with both local and remote I/O. Thus, it is possible to develope programs and use a mixture of local and remote I/O subsystems without special consideration for either.

Functional I/O Modules

The functional I/O module used in the ICS and ICR is a single hex size module and includes logic and signal conditioning.

Connection of field signals to an I/O module can be accomplished using a screw terminal assembly mounted in the system cabinet. This assembly connects to the module backplane and makes connection with the I/O module when the module is plugged into the file box. The module connector part of the assembly is offered as an option for installation where screw terminals are not required.

TYPE	DESCRIPTION
DC Inputs	Isolated DC Sense
	Isolated DC Interrupt
	Non-isolated DC Sense (TTL Compatible)
	Non-isolated DC Interrupt (TTL Compatible)
DC Output	DC Flip Flop Driver
	DC Single shot Driver
Counter	I/O Counter
AC Inputs	Isolated AC Sense
	Isolated AC Interrupt
AC Outputs	AC Flip Flop Output
	AC Single shot Output
Relay Outputs	Latching Relay Output
	Flip Flop Relay Output
Analog Input	8 Channel Analog to Digital Converter
	16 Channel Multiplexer
Analog Output	4 Channel Digital to Analog Converter

Supporting Software

The ICS and ICR are fully supported by DIGITAL's advanced family of real-time operating systems: RSX-11D, RSX-11M, and RSX-11S. The RSX operating systems offer a wide range of capabilities from stand-alone run-only multiprogramming to disk based multiprogramming with multi-user and batch processing capabilities and a choice of five programming languages. The FORTRAN user has at his disposal a full complement of process I/O subroutines for use with the ICS and ICR including the complete set of ISA standards.

The ICS is also supported by Industrial BASIC extensions available for DIGITAL's single user real-time operating system RT-11. Industrial BASIC/RT-11 is an easy to use language which utilizes simple English statements and familiar mathematical notations to perform an operation. Industrial BASIC/RT-11 includes the CALLable process I/O subroutines for use with the ICS.

PDP-11

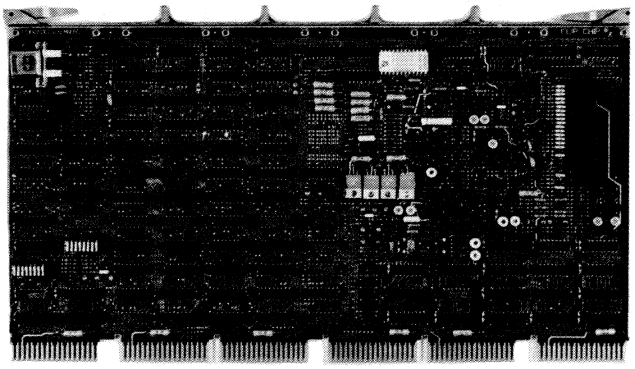
AR11 Analog Real-Time System

digital

JULY 1976

The AR11 is a compact analog real-time system that includes a 16 channel single-ended 12-bit A/D converter, a programmable real-time clock, and a scope control with dual 10-bit D/A converters. The AR11 can accept analog signals from laboratory systems and convert them to digital values recognized by the PDP-11 software.

The AR11's real-time clock can be used to acquire time interval data. In addition, operation and selection of functions is under software control.



FEATURES

- 10-bit A/D converter
- Two 10-bit D/A converters
- Display controller
- 16 channel multiplexer
- Programmable real-time clock
- A single hex-size module

DESCRIPTION

A/D Converter System

The 10-bit A/D converter samples analog data at specified rates and allows the program to store the equivalent digital value for subsequent processing. Sample and hold cicuitry ensures accurate conversions, even on rapidly changing signals, by holding the input voltage constant until the process is completed. The maximum throughput rate for a single channel is approximately 35 kHz. A 16-channel single-ended multiplexer is included. The input voltage range is program selectable for unipolar (0V to +5V), or bipolar (−2.5V to +2.5V) operation.

Display Control

The display control displays data in the form of a 1024 by 1024 dot array. Under program control, a bright dot may be produced at any point in this array. A series of these dots may be programmed to produce graphical output. The display control is primarily used with DIGITAL's VR14 display. However, it has the capabilities to operate with the Tektronix 602 and 604 display scopes and the 603, 611, and 613 storage scopes. It can also drive an X-Y analog recorder. The display control offers four program-controlled modes in which the scope can intensify a point. There are two 10-bit D/A converters with either a ±5V or a ±0.5V full scale output and all the necessary circuitry for scope control.

Programmable Clock

The programmable clock offers several methods for accurately measuring and counting time intervals or events. It can be used to synchronize the central processor to external events, count external events, measure intervals of time between events, or provide interrupts at programmable intervals. It can be used to start the A/D converter at predetermined intervals or from an external logic input.

The clock operates in one of two program modes: single interval or repeated interval. There are seven programmable frequencies: 1 MHz to 100 Hz, an external input, and an auxiliary input (on the backplane wiring).

An 8-bit counter can be preset for a number of time pulses or events to occur before an interrupt (or A/D counter start is initiated. This counter can be read from the processor at any time to determine timing status.

SPECIFICATIONS

A/D converter resolution	-10 bits
Number of input channels	-16 single-ended
Sample and hold circuits	-1
Scope control	-1024 x 1024 dot array
Scope controlled	-VR14, Tektronix scopes including storage scopes
Programmable clock rates	-7

PDP-11
LPS11 LABORATORY PERIPHERAL SYSTEM

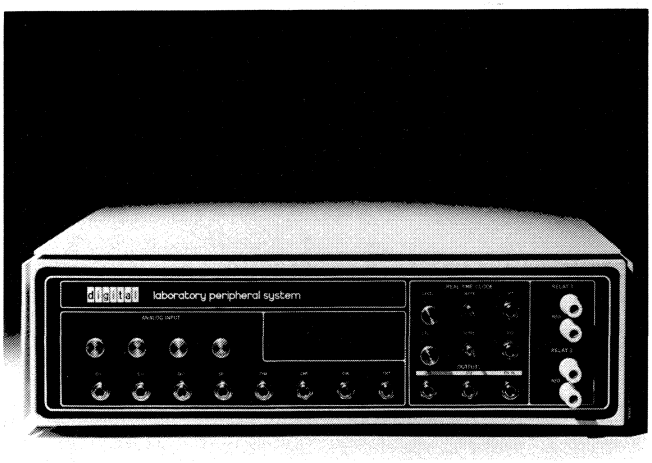
JULY 1976

The Laboratory Peripheral System (LPS11) is a high-performance, modular real-time system which interfaces a wide variety of instrumentation to PDP-11 computers. The system is supported by standard DIGITAL software, including:

- FORTRAN IV/RT-11, RSX-11D, RSX-11M
- BASIC/RT-11, CAPS
- FOCAL/RT-11
- Laboratory Application Software/RT-11
- Laboratory Application Software/CAPS-11

The system can include:

- 12-bit A/D converter
- programmable real-time clock
- display controller
- 16-bit digital I/O option
- direct memory access option



FEATURES

- 12-bit A/D converter
- Two 12-bit D/A converters
- Display controller
- Up to 64 analog input channels and 10 analog output channels
- Programmable real-time clock
- 16-bit digital I/O option
- Extremely good software support
- Digital I/O capable of word or stimulus input

DESCRIPTION

A/D Converter System

- Sample and hold circuitry
- Dual sample and hold option
- DMA option
- 8-channel multiplexer
- Optional expansion multiplexer
- Light emitting diode (LED) display
- Differential preamplifier option

The 12-bit A/D converter subsystem permits the sampling of analog data at specified rates with equivalent digital values stored for future processing. Sample and hold circuitry ensures accurate conversions, even on rapidly changing signals. The throughput rate for a single channel is approximately 40 kHz.

An 8-channel multiplexer provides eight single-ended ±5 volt inputs. Four channels are connected to phone jacks on the front panel and to potentiometer controls. The other four channels permit direct interfacing with the laboratory equipment. An 8-channel expansion multiplexer option (LPSAM) may be added so the LPS11 can handle a total of 16 channels.

Programmable Real-Time Clock

- 6 programmable frequencies
- 4 programmable modes of operation
- 2 Schmitt triggers
- Concurrent operations

The Programmable Real-Time Clock offers the user several methods for accurately measuring and counting intervals or events. It can be used to synchronize the central processor to external events, count external events, measure intervals of time between events or provide interrupts at programmable intervals. It can be used to start an analog to digital converter with the overflow from the clock counter or from the firing of a Schmitt trigger. Many of these operations can be performed concurrently.

The clock will operate in any one of four programmable modes: single interrupt, repeated interrupts, external event timing, and event counting from zero base.

The user can choose from five programmable frequencies: 1 MHz, 100 kHz, 10 kHz, 1 kHz, or 100 Hz. The real-time clock also provides an external (Schmitt trigger) input and a line frequency input.

Included with the real-time clock are two Schmitt triggers with front panel slope and level-adjusting knobs. The Schmitt triggers can start and read the clock, start the A/D converter, and cause program interrupts.

Display Control

- 4096_{10} By 4096_{10} dot array
- "Fast intensification enable" feature
- 4 program-controlled modes

The display control will display data in the form of a 4096-by-4096-dot array. Under program control, a bright dot may be produced at any point in the array. Graphic output is produced by programming a specified string of these dots. The display control is primarily used with DIGITAL's VR17 display. However, it can operate with Tektronix display scopes or storage scopes.

The display control offers four program-controlled modes in which the scope can intensify a point. In addition, the "fast intensification enable" feature permits X or Y register values to be changed by a small increment without a long scope-setting time–a feature useful in developing software character generation.

OPTIONS

The LPSAG option implements four channels with preamplifiers and provides a ±1 volt differential input to the preamplifier-implemented channels. Ranges of 0 to 2, ±5, and 0 to 10 volts are optionally available.

A direct memory option (LPSAD-NP) allows converted data to be stored in memory without processor intervention. Buffer size and location within memory can be user specified. This option frees the central processor for other tasks until an interrupt indicates the buffer has been filled.

The digital I/O option (LPSDR-A) consists of a 16-bit buffered input register and a 16-bit buffered output register. This I/O option features two program-controlled relays which are normally left open. These relays allow convenient control of laboratory equipment such as recorders, oscillators, lamps, motors and general instrumentation.

The input register may be used in two modes: as a 16-bit word transfer register or, as a monitor to cause interrupts when any one of the 16 lines changes state from +3 to ground.

The LPS switch gain multiplexer option (LPSAM-SG) is a high-performance multiplexer and amplifier that enables the LPS for low-level, wide dynamic range as well as high data rate analog conversion requirements. Signals that exceed the 4096: 1 (12-bit) dynamic range of the standard LPS ADC or simply require high accuracy at low signal levels may now be digitized with 12-bit resolution over a dynamic range of 131 040:1 and operate at up to 25 kHz sampling rate. This is obtained by using a unique approach to program-controlled, four-level gain ranging.

Each LPSAM-SG multiplexer implements eight channels with program-controlled gain; up to 16 channels can be implemented. They are installed in place of the standard multiplexers.

The LPS11-E expander enables the LPS user to extend the standard limits of 16 analog input channels and two analog outputs (DAC's) to up to 64 input channels and 10 DAC's.

SPECIFICATIONS

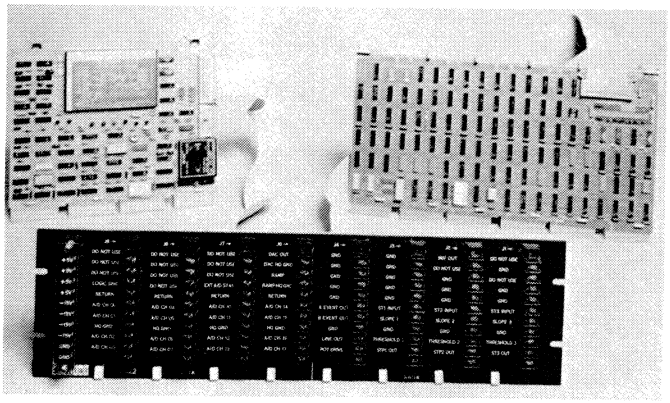
A/D converter resolution	12 bits
Number of analog input channels	8 to 64
Sample and hold circuits	1 to 2
D/A converter resolution	12 bits
Number of D/A channels	2 to 10
Scope control	4096 by 4096 dot array
Programmable clock rates	7

PDP-11 ADK11-KT Analog Real-Time Data Acquistion Package

JULY 1976

The ADK11-KT real-time analog data acquisition package is a low cost 12-bit A/D converter that accepts analog signals from laboratory systems and converts them to digital values recognized by PDP-11 software.

The ADK11-KT has a dual programmable real-time clock which provides great flexibility in timing intervals.



FEATURES

- 12-bit A/D converter
- 16 channel multiplexer
- Dual programmable clock
- Self test features which use a built-in 8-bit DAC
- Cables and H323 distribution panel included

DESCRIPTION

The ADK11-KT package consists of the necessary logic and hardware for interfacing to laboratory analog instrumentation. The package contains a 12-bit 16-channel single-ended (or 8-channel differential) analog-to-digital converter, a dual programmable real-time clock, and a distribution panel to provide a complete instrumentation interface package. Programming is software compatible with existing A/D equipment. All the time-tested software presently developed for existing analog-to-digital converters and clocks also operates with the ADK11-KT. A full range of software supports this package, such as RT-11, LA-11, and RSX-11M.

AD11-K Analog-to-Digital (A/D) Converter

The 12-bit A/D converter can be switch selected to operate as a 16-channel single-ended, 16-channel pseudo-differential or 8-channel true differential A/D converter. The A/D converter will convert an analog voltage from within one of the specified input ranges of ±5V, ±5.12V, ±10V, ±10.24V, 0 to 10V, or 0 to 10.24V to digital number for processing. These input ranges are jumper selectable. The AD11-K contains an input multiplexer, sample-and-hold, 12-bit successive approximation A/D converter and UNIBUS interface logic. The A/D converter can be started in one of three ways: under program control, on overflow of the KW11-K programmable clock, or from an external input. This versatility allows the adaptation of the package to most individual applications.

KW11-K Programmable Clock

KW11-K is a dual programmable real-time clock which interfaces directly with the UNIBUS. The first clock (clock A) is program compatible with the LPSKW clock in the LPS11.

Clock A is a 16-bit clock which can be program selected to operate at eight clock rates: five rates are crystal controlled frequencies (1 MHz, 100 KHz, 10 KHz, 1 KHz, and 100 Hz); the remaining three rates are an external (Schmitt trigger one) input, line frequency or the overflow of the second clock (clock B).

Clock A operates in one of four programmable modes of operation: single interval, repeated interval, external event timing and external event timing from zero base.

Clock B is an 8-bit programmable real-time clock which can accurately count intervals of time or events. Clock B can be used to generate a program controlled interval or to provide an input frequency for clocking clock A.

Clock B operates in repeated interval mode. Seven clock rates can be program selected: five rates by crystal controlled frequencies (1 MHz, 100 KHz, 10 KHz, 1 KHz, and 100 Hz); the remaining two rates are line frequency and external (Schmitt trigger three) input.

The Schmitt triggers for the KW11-K have both slope selection and threshhold control provided on the modules. These features are controlled by switch selection and potentiometer adjustment respectively.

H322 Distribution Panel

The H322 is a rack-mountable, general purpose distribution panel. It consists of two 40-pin Berg connectors, nine 10-screw terminal strips, two Mate-N-Lock connectors, and three double faston tabs.

The H322 contains two identical sections. One section is interfaced by BC08R cable to the AD11-K and the other section is interfaced by BC08R cable to the KW11-K. Signals from user devices can easily be interfaced using the screw terminals of the H322. A decal set for the AD11-K and KW11-K is used to identify each terminal.

All screw terminals can be utilized by simply stripping the end of the wire from a device, placing the wire under the screw terminal lug and tightening the screw. No soldering or access to the interior of the system is needed.

SPECIFICATIONS

A/D converter resolution	12 bits
Number of input channels	16 single-ended or 8 differential
Sample and hold circuits	1
Programmable clock rates	
Clock A	8
Clock B	7

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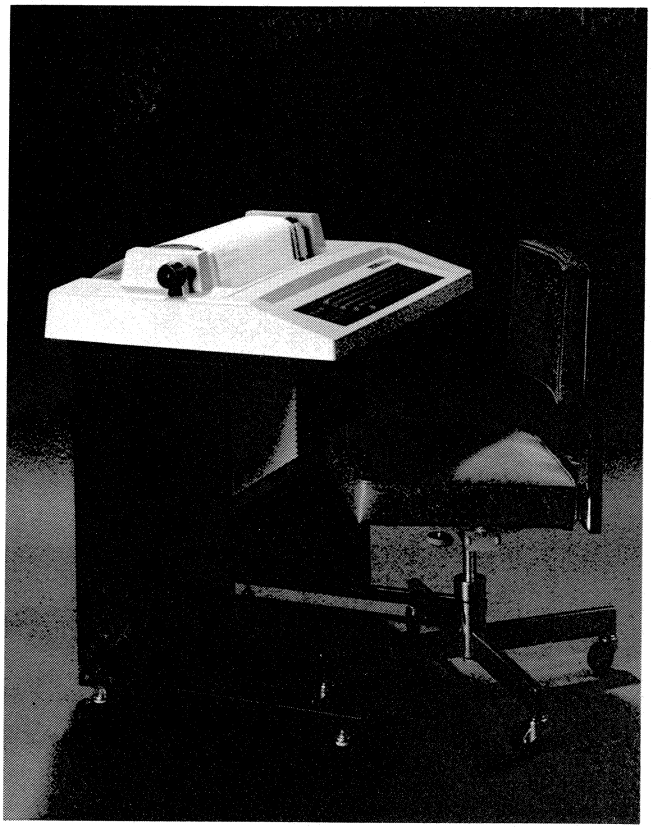
PDP-11

LA 36 DECwriter II

digital

JULY 1976

The LA36 DECwriter II is designed to be industry's lowest-priced, best performing, most reliable 30-cps impact teleprinter. DECwriter II is packed with capability: it's fast—a true 30-cps machine; it's quiet—you'll almost forget it's there; it has many people-oriented design considerations you wouldn't expect in a cost-conscious product; it's versatile—you can use 6-part forms and even standard 132-column line printer paper; and it's built for a long, reliable lifetime of heavy use.



FEATURES

- True 30-character per second throughput
- Accommodates 6-part form (.020 maximum thickness)
- Handles variable width forms, 3″ through 147/8″ wide
- 132-column printing, 10 characters per inch horizontal
- 6 lines per inch vertical spacing
- 128-character ASCII upper/lower case set
- 7 x 7 dot matrix
- Integrated, 20ma current loop interface with jumpers for active and passive modes
- EIA interface with modem control

Human Engineering

- ANSI-standard typewriter-like keyboard
- Quiet operation
- Excellent character readability
- Fine vertical adjustment for accurate forms placement
- Paper out sensor
- Print window, column scale, and pointers
- 14-key numeric pad
- Paper stacking tray

DESCRIPTION

The LA36 DECwriter II is a second generation machine which feature for feature is the most cost competitive in the industry. DECwriter II offers fast, reliable operation and is extremely easy to interface as a remote terminal, local computer I/O device and many other related applications.

DECwriter II is loaded with many practical functional and operator features. Among these are 30 cps throughput accomplished by a 60 cps catchup mode which is activated any time that more than one character is in the 16 character buffer. Also featured are quiet operation, infinitely variable vertical forms adjustment, variable forms width, and multi-part forms capability.

The typewriter-style keyboard assures easy operator adaptation. The 7-wire print head is designed to have the longest life in the business and produces extremely clear character definition.

Operation

Seven solenoid driven wires form the characters by scanning the page from left to right. The scanning motion is servo controlled. Upon command, stepping motor controlled line feed is actuated.

Power up

Upon power up the DECwriter II is initialized to execute incoming data. The carriage first moves to the right, then reverses until it is stopped by the left bumper. It then moves 0.2 inches to the right which establishes the position of column 1. This sequence is only entered upon power up.

Carriage System

The carriage system transports the head along the horizontal axis of the machine and provides accurate horizontal positioning for character placement and precise print gap and adjustment for clean impressions on a variety of forms.

The carriage is controlled by a servo system which enables accurate dot placement. The servo operates in the forward direction at 3 and 6 inches per second. The 3 ips speed is the normal mode while the 6 ips speed is used for catch up due to carriage return and worst case printing condition where the printer might fall behind at 3 ips.

Ribbon Feed System

The ribbon feed system is driven by the carriage motion only when the carriage is moving from left to right. This prevents ribbon smudging when the DECwriter is not printing.

Paper Feed System

The paper feed system is a stepping motor driven tractor feed. The tractor design provides 3 to 4 pins engagement of the form and a flat bed for control and positive feeding of multipart paper. Paper may be fine positioned vertically by pushing the line feed knob inward and rotating it in the direction desired.

770526

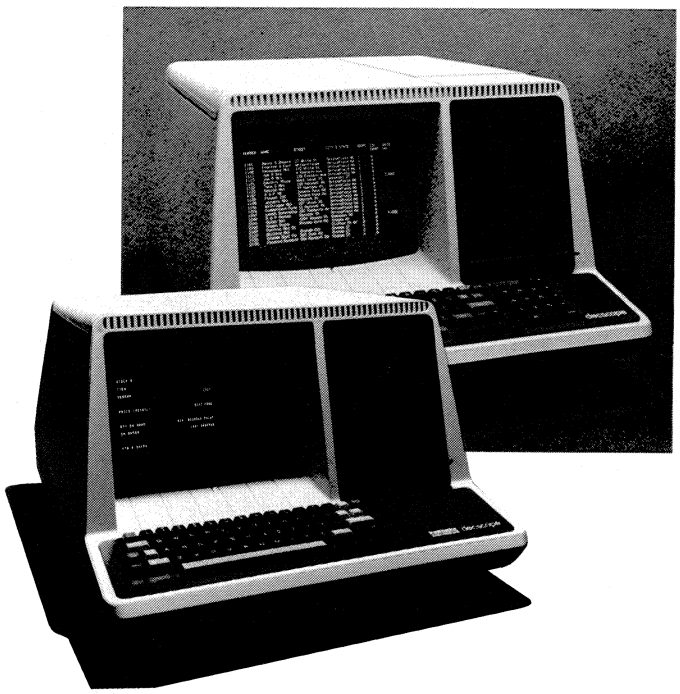
PDP-11

DECscope Video Terminals

digital

JULY 1976

DECscopes—DIGITAL's VT50 series of character oriented video terminals—eliminate the need for electromechanical devices. They are all simple for operators to master, quieter than mechanical terminals, and inexpensive. The three models—VT50, VT50H, and VT52—differ only in advanced application features.



FEATURES:

Human Engineering

- Typewriter-like keyboard layout makes it easy to learn
- Audible keyclick further reinforces the feel of normal typewriter operation.
- Multiple rollover eliminates errors that might occur due to fast typing: up to three keys can be depressed and transmission will be correct if one of the first two is released before the third.
- Fixed horizontal tabs aid formatting
- Quiet operations result from the elimination of cooling fans
- The screen is designed for readability. Character brightness is operator-adjustable and the screen is recessed and tilted to avoid glare from overhead lighting.
- The standard DECscope has no filter covering the screen so it can be easily cleaned by the operator, but for users with special applications, the DECscope is designed to accept colored filters.
- Hold screen mode allows the operator to control the flow of data. At high baud rates this is significant since scrolling (movement of lines up the screen) can occur so rapidly that visual inspection is impossible.

Power

- 19 key auxiliary numeric keypad requires no reprogramming (VT50H and VT52)
- Alternate mode for key pad allows each of the 19 keys to be uniquely recognizable (VT52)
- 3 user defined function keys (VT50H and VT52)
- Functions implemented using AINSI standard escape sequence protocol provides for future expansion
- Cursor control keys (VT50H and VT52)
- Direct cursor addressing (VT50H and VT52)
- Upper and lower case characters (VT52)
- Terminal prevents data overflow by signalling software to suspend (XOFF) transmission and resume (XON) when ready
- Optional printer interface allows terminal to output copy to printer (VT52)

Range

- 75-9600 baud with switch selectable split transmission and reception rates
- 12 or 24 lines of 80 characters each
- Full duplex, full duplex with local copy

Cost Effectiveness

- Low initial price which is comparable to slow teletypewriters
- Minimal maintenance costs since the simplified mechanics (no moving parts except for the keyboard and the key-click system) give the DECscopes built-in reliability
- Minimal installation cost and effort due to the elimination of cabling restrictions and the use of a built in self test feature
- Faster baud rates (up to 9600 baud) lowers the cost of moving data

FEATURE COMPARISON CHART

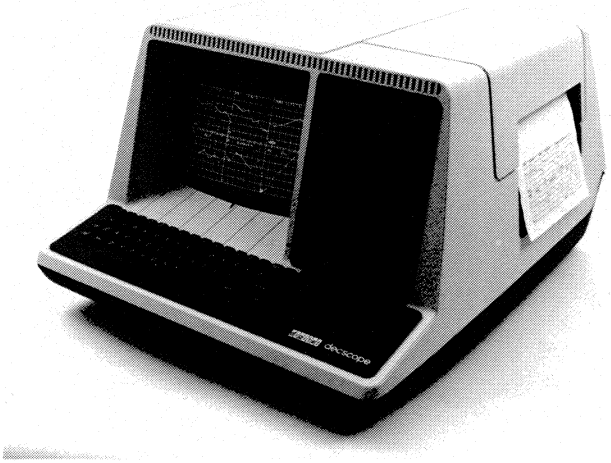
	VT50	VT50H	VT52
Screen Format	12 lines x 80 characters	12 lines x 80 characters	24 lines x 80 characters
Char. Matrix	5 x 7	5 x 7	7 x 7
Char. Set	64 ASCII upper case	64 ASCII upper case	96 ASCII upper and lower case; 32 special graphic characters
Cursor Control	Cursor movement by escape sequence	Direct cursor addressing plus individual cursor control keys	Same as VT50H
Keyboard	Standard typewriter layout	Standard typewriter layout plus 19 keypad (11 numerics, 4 cursor keys, 3 user definable function keys, ENTER key) plus auto repeat key.	Same as VT50H plus a special application mode on the 19 key pad
Communications	20ma standard; EIA optional	20ma standard; EIA optional	20ma or EIA standard
Baud Rates	75-9600 baud split baud rates switch selectable	Same as VT50	Same as VT50
Other Features	Upward scroll	same	same
	Erase to end of line	same	same
	Erase to end of screen	same	same
	Hold Screen Mode	same	same
	Fixed Tabs	same	same
			Downward scroll

PDP-11
VT55 Graphics Terminal

digital

JULY 1976

The VT55 is an on-line interactive CRT terminal that offers waveform graphics capability–a new and significant extension to meet the needs of a variety of applications. Two graphs of 512 (maximum) data points each can be displayed with a screen resolution of 512 x by 236 y. Cursors (20-point vertical lines) are available (one per data point) to facilitate data editing and graph generation. In addition, the VT55 allows simultaneous display of any combination of text graphics. By simply pressing a specified key, the VT55 supplies a hard copy reproduction of the display screen for both characters and graphs. In essence, then, it is three devices in one–an alphanumeric terminal, a graphic drawing terminal and a printer/plotter.



FEATURES

Alphanumeric Terminal

- Upper and lower case ASCII
- Direct cursor addressing in alphanumeric and special character mode
- Set of special characters which may be displayed on the CRT and printed on the copier.
- Separate numeric keypad
- User-defined codes generated from keypad
- 7 x 7 point character font
- REPEAT key on the keyboard
- Downward and upward scroll
- 24 lines of 80 columns/line
- Line speeds of 75–9600 baud
- Full or half-duplex
- 20 mA interface

Graphic Drawing Terminal

- Two graphs can be drawn (two y values for every x)
- Each graph can be point-plot or histogram
- x values from 0-512; y values from 0–236
- Markers (short vertical bars) can be attached to any point.
- Vertical and/or horizontal grid lines can be placed at any position.

Hard Copy Unit

- Very low cost
- Electrolytic process
- Simple to operate (push button)
- Auto-copy capability (line by line)
- 25 seconds for full screen development
- Four cents/copy

DESCRIPTION

Waveform graphics capability is an important addition to applications involved with such activities as plotting histograms, waveform and peak analyses, data acquisition, monitoring, trending, simulation, laboratory charts and forms . . . wherever results can be improved through graphics with extended capability.

The VT55 Screen

The screen is tilted to avoid glare from overhead lighting. A control at the rear of the terminal allows the operator to adjust screen brightness for the best possible vision under varying light conditions. The standard model has no filter covering, so it can be easily cleaned.

Operator response to the VT55 is based on the cursor–a flashing underline that indicates where the next character will appear. Because it is a fast position indicator, the cursor encourages quick operator response. (Programs can also direct the computer to display a form on the screen and move the cursor to its proper location so the operator can fill in responses.)

The cursor provides a full range of user control flexibility, including both conventional and extended-movement commands utilizing escape sequences. Up, down, right, and left movements, plus 8-space tabbing are available.

The full screen as well as individual characters and lines can be erased by using simple "ESCape" commands (an escape character followed by another character). Line speeds of up to 9600 baud allow high-speed display of and interaction with the terminal's character and graphic displays.

At high baud rates, the operator can freeze data transmission with the SCROLL key. When the bottom line of text on the screen is displayed, and the cursor is directed to move to the next line, the top line of text automatically "scrolls" off the screen to allow space for the new line.
When receiving data at high baud rates, this scrolling can occur so rapidly that a visual inspection of screen information is impossible. The VT55 allows scrolling to be controlled at the terminal. When the screen is full, transmission stops until the SCROLL key is pressed, signalling that the operator is ready to proceed.

Two control dials let the operator select transmission rates from 75 to 9600 baud (75, 110, 150, 300, 600, 1200, 2400, 4800, and 9600). These controls can be set separately so that some reception and transmission speeds can be mixed.

The VT55 Copier

The electrolytic copier, located on the side of the terminal, prints line-for-line images of the text and graphics that are displayed on the screen.

To copy all lines currently on the screen, the operator simply presses the COPY key. The terminal tells the host computer to wait (sends XOFF code) and normal operations will resume after the copying is done (terminal sends XON code). This operation can also be initiated by the computer program.

The VT55 Keyboard

The VT55 keyboard is built to a universally accepted standard–the office typewriter. Its layout, stroke and touch are familiar to any typist, thereby maintaining the training and familiarization period to an absolute minimum, without sacrificing accuracy and speed.

The VT55 keyboard features multiple-key rollover construction that encourages operator speed by eliminating errors due to striking multiple keys.

VT55 Software

A set of simple FORTRAN/BASIC CALLS is provided to allow easy use of the graph drawing facilities:

- –Load graph 1 or graph 2
- –Specify starting x coordinate and series of y values
- –Alter mode (alphanumeric/graphic; point plot/ histogram)
- –Set or erase markers
- –Set or erase grid lines

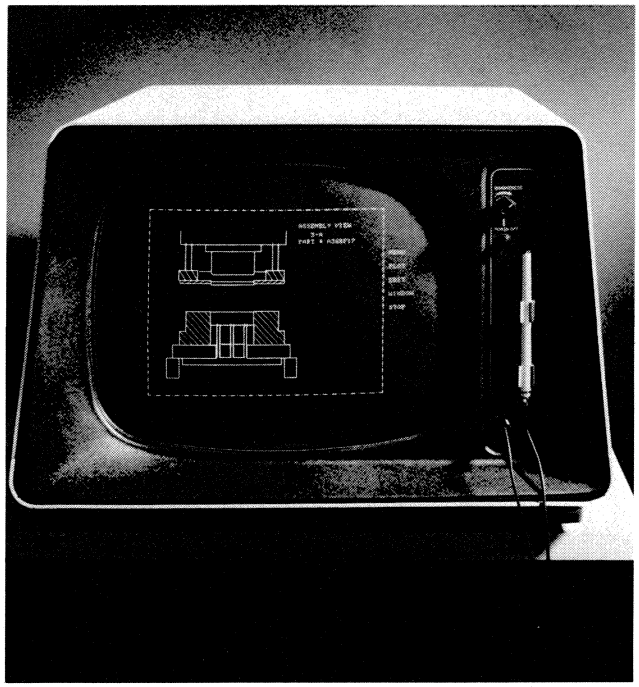
FOCAL/RT-11. FOCAL/RT-11 is a powerful interactive high level programming language designed for applications which require simplicity as well as the full problem solving capabilities of a general purpose digital computer. FOCAL support of the VT55 is similar to BASIC but is implemented by using the "FNEW" feature. FOCAL is particularly well suited to one-time calculations and offers a full range of mathematical functions, extendable I/O, and versatile self-editing capabilities. The basic FOCAL command set contains 12 powerful commands which are all that is required for most applications.

PDP-11
VT11 Graphic Display Processor

digital

JULY 1976

The VT11 graphic display subsystem is a direct memory access, refresh display processor with a 17 inch CRT and light pen. It provides all the basic tools needed to add a graphics capability to an existing PDP-11 processor. The VT11 includes the video display, interface and display processor. These are provided for the user who wishes to add graphics capabilities to a PDP-11 system.



FEATURES

- Hardware character generation
  Full ASCII character set plus 31 special symbols.
  Italics for all characters and symbols.
- Hardware vector (line) generation:
  Relative short vectors
  Relative long vectors
  Four line types—solid, long dash, short dash, and dot dash
- Hardware point generation:
  Absolute X, Y points
  Relative X, Y points
  Special graph plotting modes
  1024 X 1024 point addressing
- Eight brightness levels
- Hardware blink
- Programmable sensitivity of the light pen for any graphic element
- Direct memory access for instructions and data
- Optional free-standing keyboard with 128 ASCII characters and eight programmable function keys
- Optional 16 button push button box which is general purpose in design, since the button functions are programmable

DESCRIPTION

Display Processor

Most of the advanced graphic-display capabilities of the VT11 are provided by the display processor. It performs all instruction fetching, data fetching, and execution of graphic commands within the subsystem.

CRT Monitor

The CRT monitor provides the graphic output for the VT11-A subsystem. It features the exceptional brightness and contrast characteristics of refreshed, electromagnetic displays. The CRT measures 17 diagonal inches and provides a viewable area of 8.25 by 11 inches.

Light Pen

The light pen is a solid state sensor that facilitates user interaction with the system. It functions as an active input to the central processor, when it is pointed at a sensitive element on the CRT.

SOFTWARE ENVIRONMENT

Since the VT11 can be added to any PDP-11 with a UNIBUS, it is supported under the following operating systems:

- CAPS-11 systems (FOCAL and BASIC)
- RT-11 single user or foreground/background (FOCAL, BASIC and FORTRAN)
- RSX-11M multi-tasking system (FORTRAN)

The software provided falls into the following categories:

1) Device drivers—incorporated into the operating system to provide basic interrupt handling and input/output.
2) Display file management—subroutines or function "CALLS" allowing the user to construct and manipulate display files (hence, images on the screen).
3) Utility functions—software to fulfill related functions, e.g., this includes the RT-11 graphics editor and LV11 display file output routines.

RT-11 Graphics Editor

In RT-11, by typing the command GT ON, the user can then use the VT11 as a screen editor. The main features are:

- 10 lines above and below current editor points displayed on screen. This is automatically re-displayed as the user adjusts the pointer position.
- A 5-line "scroller" area at the bottom of the screen holds input/output which would normally go to the console, e.g., editor commands.

RT-11/LV11 Plot Routines

Since the LV11 printer/plotter is often used as a hard copy output for VT11 display files, we have provided software features to do this in the LV11 plotting package (an RT-11 optional extension).

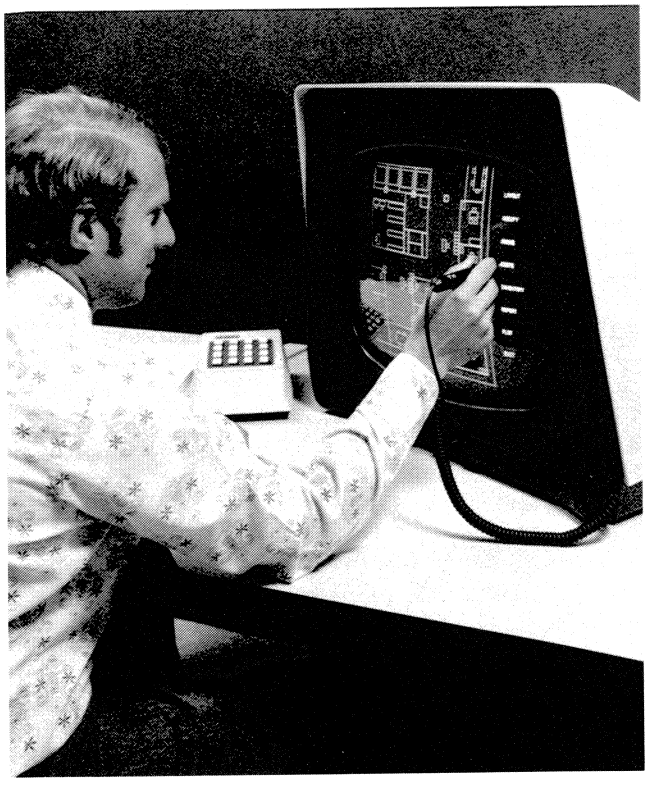
MÅN PROGRAMMET

PDP-11
VS60 Graphic Display Processor

digital

JULY 1976

The VS60 graphic display processor is a high performance analog stroke system with a 21-inch CRT screen, a light pen and a sophisticated graphic display processing unit. This display processor includes such advanced features as windowing, scaling, and two-dimension rotation.



FEATURES

Quality
- Stroke vector generator
- Stroke character generator

Efficiency
- Direct memory access
- High speed processor
- Parallel processing

High Performance Capability
- Scaling
- Windowing
- Subpictures
- Naming and associative searching

Flexibility
- 4 line types
- 2 CRTs
- 8 intensity levels
- Refresh display with light pen
- Blink
- Full ASCII character set and special graphics symbols
- Sub and super scripts
- 90% rotation
- Separate menu
- Light pen with tip switch

Description
The VS60 graphic unit is a high-speed analog stroke system which drives a 21-inch (53 cm) CRT and comes complete with a light pen. It is a refresh device which accesses its picture commands from a PDP-11 memory and communicates with a PDP-11 both through the use of interactive devices and through programmed interrupts.
As an instruction-compatible upgrade to the VT11, the VS60 has such standard features as hardware vector and character generators, eight intensity levels, four line types, and blink.

In addition, many sophisticated graphic features previously found only as expensive add-ons to high-end graphic units are standard. Among these are super and subscript characters, hardware scaling, windowing, subroutining with automatic stacking, and the ability to drive two independent CRTs.

Display Processing Unit
The DPU functions in a manner similar to the central processor. Fetching both graphic instructions and graphic data from the PDP-11's memory, it operates on the information and draws the corresponding picture image on the CRT.

Modes

The VS60 has nine graphic modes for drawing lines, points and text on the CRT. There are also many higher level instructions which make the graphic processor a truly interactive device.

Lines may be represented in five different data formats: long relative vectors, short relative vectors, absolute vectors, plus long and short "basic" vectors.

Points are specified in one of three formats: absolute, relative, and graphplot mode.

The text mode is stored in one data format consisting of two 7-bit values per word. Different escape sequences are used to display the 31 special symbols as well as super and subscripting.

Subroutines

In many applications, combinations of points, lines, and text form special symbols which are repeated many times in the total picture. Through the use of graphic subroutine calls, the user can define a graphic symbol as a subpicture and call the subroutine each time the symbol is to be repeated.

Direct Memory Access

In order to refresh the CRT, the display processor must have the ability to directly address the PDP-11's memory. This addressing is accomplished through the display processor's program counter, which operates in a manner analogous to the computer's program counter; the DPU program counter automatically increments through the display file allowing access to sequential picture data.

GT62 Graphic Display Terminal

The GT62 is a high performance graphic display terminal which combines the PDP-11/34 and a VS60. It includes a programmer's console, a 16-button function key pad, and an ASCII keyboard. This terminal is supported by RSX-11M and RSX-11D.

Fortran Support

DECgraphic-11 FORTRAN support is a package of graphics subroutines for the FORTRAN user of the VS60. Through its comprehensive set of subroutine calls, it allows the user to display, modify, and interact with graphical information at the display console. The routines support the DECgraphic-11 display processor as a UNIBUS peripheral to the following operating systems:

- –RT-11 (dedicated or foreground/background)
- –RSX-11M (multitask environment)

DECgraphic-11 FORTRAN support includes:

1. Device handlers for the appropriate operating system.
2. A set of library modules for the FORTRAN library.

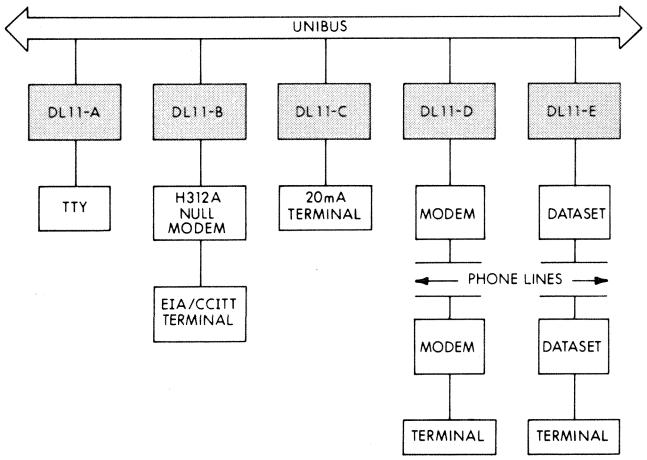
The complete set of library modules includes some 60 FORTRAN callable subroutines.

PDP-11

DL11-W Serial Line Asynchronous Interface

JULY 1976

The DL11-W connects the PDP-11 UNIBUS with an asynchronous serial communications line. It is a low-cost, flexible unit which can be used with local, leased or dial-up lines. In addition it is a line frequency clock which can provide timed interrupts, allowing a program to measure passage of time.



FEATURES

Flexibility

- Contains a line frequency clock
- Character sizes of 5, 6, 7 or 8 data bits
- Even, odd or no parity
- Stop code lengths of 1, 1.5 or 2 bits
- Split transmit/receive speeds
- Leased line or dial-up modems
- Full or half duplex transmission

Speed

- Up to 9600 baud

DESCRIPTION

The DL11 is an interface between a single asynchronous serial communication channel and the PDP-11. It performs serial-to-parallel and parallel-to-serial conversion of serial start-stop data with a double character buffered MOS/LSI circuit called a UART (for Universal Asynchronous Receiver-Transmitter). This 40-pin dual-in-line package includes all of the circuitry necessary to double buffer characters in and out, serialize-deserialize data, provide selection of character length and stop code configuration, and present status information about the unit and each character.

With a DL11 interface, a PDP-11 computer can communicate with a local terminal such as a console teleprinter, with a remote terminal via data sets and private line or public switched telephone facilities, or with another local or remote PDP-11 computer.

DL11 systems provide wide flexibility. The user can specify data rate from a selection of 13 standard rates between 40 and 9600 Baud, or he can order a non-standard rate device. With most of the standard rates, the interface can offer split-speed operation for faster, more efficient handling of computer output.

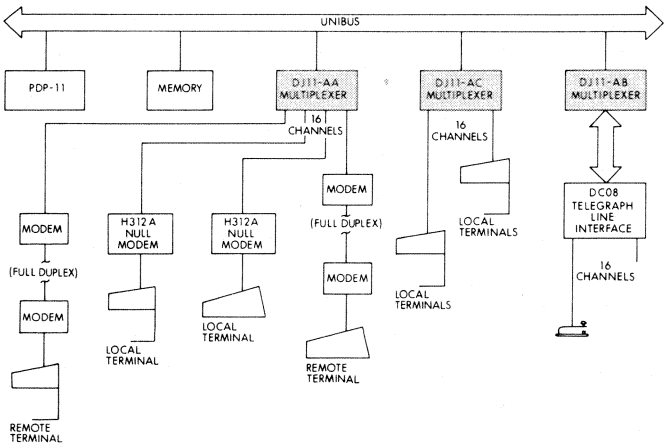
For additional flexibility, character size is strap selectable for 5, 6, 7, or 8-level codes. Also strap selectable are parity checking (even, odd, or none) and stop code length (1, 1.5, or 2 bits).

PDP-11

DJ11 Asynchronous Serial Line Multiplexer

JULY 1976

The DJ11 multiplexer connects the PDP-11 UNIBUS with 16 asynchronous serial communications lines. The DJ11 is a low-cost, medium performance unit whose character formats and operating speeds are jumper or switch selectable in groups of four lines.



FEATURES

Speed

- Each line of the DJ11 may run at jumper or switch selectable speeds up to 9600 baud

Flexibility

- Character Size–5, 6, 7 or 8 bits
- Stop Code Length–1, 1½ (5-bit data only) or 2 bits
- Transmission Mode–full duplex or half-duplex
- Parity–three configurations generated and checked by the hardware

Capacity

- 64-character hardware buffer for received characters
- Up to 256 lines per PDP-11

DESCRIPTION

DJ11 is an economical interface for connecting the PDP-11 to terminals of modems in 16-line groups. Such features as total number of data bits, stop bits, parity bit, split speeds and full- or half-duplex are switch-selectable. There are 11 standard speeds up to 9600 baud to choose from. 20 mA and EIA/CCITT models are available. The DJ11 contains a 64-character "silo" buffer for received characters.

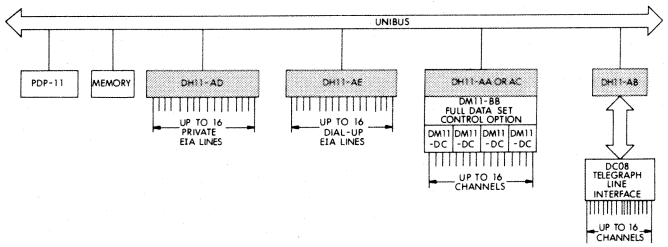
The DJ11 performs serial-to-parallel and parallel-to-serial conversion of serial start-stop data with double character buffered MOS/LSI circuits called UART's (Universal Asynchronous Receiver Transmitters). These circuits provide the logic necessary to double buffer characters in and out, to serialize-deserialize data, to provide selection of character length and stop code configuration, and to present status information about the UART and each character. A 64-character, first-in/first-out buffer is provided in the hardware to hold characters as they are received.

PDP-11 DH11 Programmable Asynchronous Serial Line Multiplexer

digital

JULY 1976

The DH11 multiplexer connects the PDP-11 UNIBUS with 16 asynchronous serial communications lines. The DH11 is a high-performance unit whose character formats and operating speeds are programmable parameters. Data is buffered on input and is transferred directly from memory.



FEATURES

Speed

- Each line of the DH11 may run at program-selectable speeds up to 9600 baud

Flexibility

- Complete program control of each line for:
  Data Rate—14 standard speeds, plus two external inputs
  Character Size—5, 6, 7 or 8 bits
  Stop Code Length—1, 1½ (5-bit data only) or 2 bits
  Transmission Mode—full duplex or half-duplex
  Parity generation and checking

Capacity

- 64-character hardware buffer for received characters
- Up to 256 lines per PDP-11

Power

- Program-controlled hardware echo of received characters
- Direct memory access transmitter for each line, with byte count and address registers in hardware
- Hardware break detection and program-controlled break generation
- Dial-up or local options

DESCRIPTION

For applications requiring large numbers of dial-up terminals, or mixing of 20 mA and EIA/CCITT connections, the DH11 series of interfaces is available. Interface characteristics (such as number of data bits, parity, etc.) are program-selectable. Thirteen speeds up to 9600 baud are available. For received character handling, the DH11 contains a 64-character "silo" buffer; for transmitted characters it contains a DMA transmitter for each line. 20 mA and EIA/CCITT connections can be mixed on one DH11 16-line unit.

Programmable Parameters:

Character length:	5, 6, 7, or 8 bits
Number of stop bits:	1 or 2 for 6-, 7-, 8-bit characters 1 or 1.5 for 5-bit characters
Parity generation and detection:	Odd, Even, or None
Operating mode:	Half Duplex or Full Duplex
Transmitter speed (Bauds):	0, 50, 75, 110, 134.5, 150, 200, 300, 600, 1200, 1800, 2400, 4800, 9600, Ext A, Ext B.
Receiver speed (Bauds):	0, 50, 75, 110, 134.5, 150, 200, 300, 600, 1200, 1800, 2400, 4800, 9600, Ext A, Ext B.

Breaks may be detected and generated on each line.

The DH11 Multiplexer uses 16 double-buffered MOS/LSI receivers to assemble the incoming characters. An automatic scanner takes each received character and the line number and deposits that information in a first-in, first-out buffer memory referred to as the "silo." The bottom of the silo is a register which is addressable from the UNIBUS.

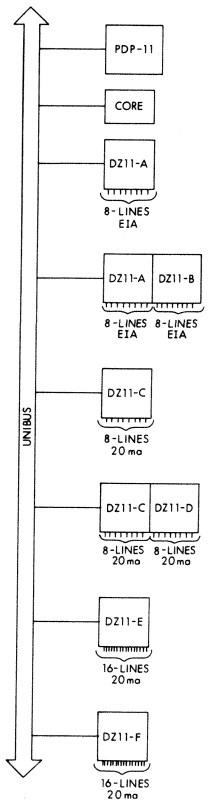
The transmitter in the DH11 also uses double-buffered MOS/LSI units. They are loaded directly from message tables in the PDP-11 memory by means of single cycle direct memory transfers. The current addresses and data byte counts for each line's message table are stored in semi-conductor memories located in the DH11. This reduces the UNIBUS time required for direct memory transfers to on direct memory cycle per character transmitted.

As many as 16 DH11's may be placed on a single PDP-11 processor, creating a total capacity of 256 lines.

PDP-11 DZ11 Programmable Asynchronous Serial Line Multiplexer

JULY 1976

The DZ11 multiplexer connects the PDP-11 UNIBUS with 8 to 16 asynchronous serial communications lines. The DZ11 is a small, low-cost, medium performance unit whose character formats and operating speeds are programmable parameters.



FEATURES

Speed

- Each line of the DZ11 may run at program-selectable speeds up to 9600 baud

Flexibility

- Complete program control of each line for:
  Data Rate—15 standard speeds, plus two external inputs
  Character Size—5, 6, 7 or 8 bits
  Stop Code Length—1, 1½ (5-bit data only) or 2 bits
  Transmission Mode—full duplex
  Parity generation and checking

Capacity

- 64-character hardware buffer for received characters
- Up to 128 lines per PDP-11

Power

- Program-controlled hardware echo of received characters
- Hardware break detection and program-controlled break generation
- Dial-up or local options

Size

- Single hex module for 8-line configuration
- Two hex modules for 16-line configuration

DESCRIPTION

The DZ11 is a single hex module together with an unpowered 5¼" distribution panel. The module supports 8 lines while the panel supports 16 lines. The DZ11 may interface any UNIBUS PDP-11 to 8 asynchronous lines at any of 15 baud rates up to 9600. Baud rates and character formats for each line are programmable on a per-line basis.

The DZ11 is available in two versions, an EIA version and a 20 mA version. The DZ11 may be used with dial-up full duplex terminals. These terminals may operate at up to 300 baud (using Bell 103 or 113 modems), or up to 1200 baud (using the Bell 212 modem). The DZ11 can also be used for private wire operation up to 1800 baud (with Bell 202 modem, full duplex). Local operation with EIA terminals without modems is possible up to 9600 baud.

The 20 mA version will interface to local 20 mA terminals. A system requiring both EIA and 20 mA operation must use multiple DZ11's.

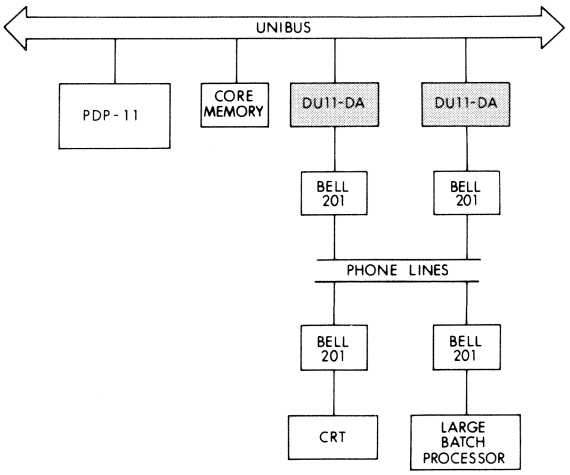
Incoming characters are silo buffered. Outgoing characters are processed on a program interrupt basis. The DZ11 can generate and detect break characters.

PDP-11

DU11 Single Synchronous Line Interface

JULY 1976

The DU11 is a single-line, program-controlled, double-buffered communications device designed to interface the PDP-11 processor to a serial synchronous line. The self-contained unit is fully programmable with respect to sync character, character length (5 to 8 bits), and parity selection.



FEATURES

- Transmission speeds up to 9600 baud
- Double-buffered program interrupt
- Full- or half-duplex operation
- Programmable sync character
- Programmable character size (5, 6, 7, or 8 bits)
- Receiving sync character stripping program selectable
- Automatic transmit of sync program selectable
- Interfaces to Bell series 200 synchronous modems or equivalent
- Auto answering capability
- Parity checking and generation
- Modem control
- Simple, compact, single-board design

DESCRIPTION

The DU11 is an economical interface for connecting PDP-11's to synchronous modems or lines. Character size, full- or half-duplex, parity checking, and full- or half-duplex operation can be selected by software transmission and speeds up to 9600 bits per second are possible. A clock option (DFC11) for PDP-11-to-PDP-11 connections without modems, and a hardware CRC/LRC option (KG11-A) are available.

The DU11 is well suited for interfacing the PDP-11 to synchronous lines for remote batch, remote data collection, and remote concentration applications. Multiple DU11's on a PDP-11 allow its use as a synchronous line concentrator or front-end synchronous controller to a larger computer.

The DU11 provides serial-to-parallel and parallel-to-serial data conversion, voltage level conversion, and modem control for half- or full-duplex operation. The Bell series 200 synchronous modems or equivalent may be used with the DU11.

Modem control is a standard feature of the DU11. The necessary signals needed to establish communications with the Bell series 200 synchronous modems are present in the receive status register (RxCSR). No transition of control lines emanating from the modem directly cause a change in the state of the transmitter or receiver logic.

The DU11 is capable of transmitting data at the following speed:

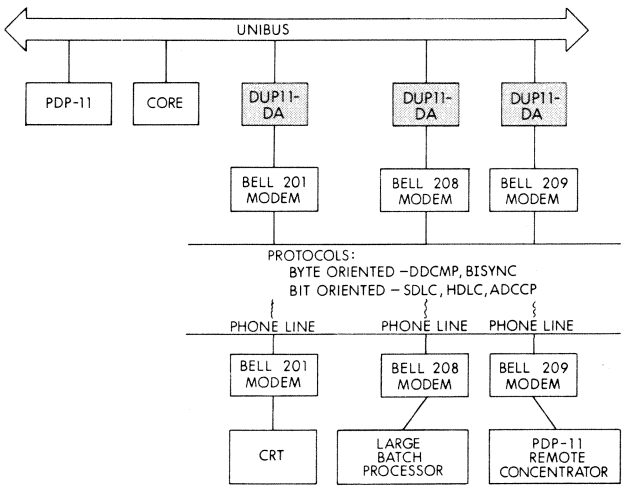
EIA/CCITT: 9600 Baud maximum
(limited by modem and data set interface level converters)

PDP-11

DUP-11 Single Synchronous Line Interface

JULY 1976

The DUP-11 is a single-line, program-controlled, double-buffered communications device designed to interface the PDP-11 processor to a serial synchronous line. The self-contained unit is capable of handling a wide variety of protocols, including byte-oriented protocols, such as DDCMP and BISYNC and bit-oriented protocols, such as SDLC, HDLC and ADCCP.



FEATURES

- Transmission speeds up to 9600 baud
- Double-character-buffered receive & transmit
- Full- or half-duplex operation
- Byte-oriented operation (protocols such as DDCMP and BISYNC)
- Bit-oriented operation (protocols such as SDLC, HDLC, ADCCP)
- CRC-16 generation and checking for use with DDCMP protocol
- CRC/CCITT generation and checking for use with bit-oriented protocols
- Programmable SYNC character for byte-oriented operation
- Secondary address recognition for bit-oriented operation
- 8-bit character size
- SYNC stripping on receive operations under program control
- Interfaces to Bell 201, 208, and 209 series synchronous modems or equivalents
- Auto answering capability
- Modem control
- Simple, compact single-board design (i.e., SPC slot UNIBUS option)

DESCRIPTION

The DUP-11 is a character-buffered, synchronous, serial-line interface capable of two-way simultaneous communications. The DUP-11 translates between serial data and parallel data. Output characters are transferred in parallel from the PDP-11 UNIBUS into the DUP-11 where they are serially shifted to the communication line. Input characters from the modem are shifted into the DUP-11 and made available to the PDP-11 on an interrupt basis.

This allows a full character time in which to service transmitter and receiver interrupts. The clocking necessary to serialize the data is provided by the associated synchronous modem.

The DUP-11 is well suited for interfacing the PDP-11 to medium-speed synchronous lines for remote batch, remote data collection, remote concentration and network applications. Multiple DUP-11's on a PDP-11 allow its use in applications requiring several synchronous lines.

Modem control is a standard feature of the DUP-11. The necessary signals needed to establish communications with the Bell Series 200 synchronous modems are present in the Receive Status Register (RxCSR). A transition of control lines emanating from the modem directly will not cause a change in the state of the transmitter or receiver logic.

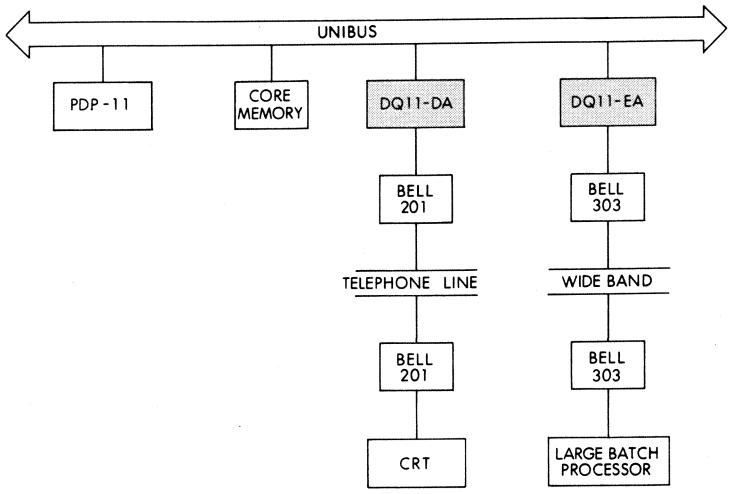
The DUP-11 is capable of transmitting data at the maximum speed of 9600 baud (limited by modem and data set interface level converters).

The DUP-11 conforms to Electronic Industries Association (EIA) specification RS232C and CCITT Recommendation V.24.

PDP-11
DQ11 Synchronous Line Interface

JULY 1976

The DQ11 is a high-speed, double-buffered communications device designed to interface the PDP-11 to a serial synchronous communications channel. This interface allows the PDP-11 to be used for remote batch and remote concentrator applications. With the DQ11, the PDP-11 can also be used as a front-end synchronous line controller to handle remote and local synchronous terminals.



FEATURES

Speed

- Transmission speeds up to 1.0 Megabaud when utilizing an appropriate protocol

Throughput

- Direct memory access data transfers for transmit and receive
- Double-buffered transmit and receive data registers
- Double-buffered character count and bus address registers

Flexibility

- Full or half duplex operation
- Programmable parity (VTC) checking. Parity (odd or event) is switch selectable.
- Data set control
- Switch-selectable (one or two) sync characters to character fram
- Programmable sync character
- Programmable character size—up to sixteen bits per character with double character transfers for characters containing eight bits or less
- Three switch-selectable control characters for program interrupts
- Interfaces to Bel 201, 208, and 303 or equivalent modems
- Optional programmable character recognition and hardware sequence control to assist protocol implementation

Reliability

- Diagnostic-controlled self-testing capabilities
- Optional internal crystal clock specified at baud rate
- Optional programmable up to 24-bit polynomial for LRC or CRC checking

DESCRIPTION

The DQ11 is a double-buffered synchronous serial line interface capable of two-way simultaneous communications. It translates between serial data and parallel data. Output characters are transferred in parallel from the PDP-11 UNIBUS into the DQ11 where they are serially shifted to the communication line. Input characters from the modem are shifted into the DQ11 and made available to the PDP-11 on a direct memory access interrupt basis.

Synchronization between the DQ11 and the transmitting device is established by a sync character code. Once synchronization is achieved, serial data can be transmitted and received continuously (no start or stop bits are required as in asynchronous communications). Both the receiver and transmitter are double buffered. Since the character count register is also double buffered, a full buffer time is available to service character count overflow interrupts. The clocking necessary to serialize the data may be provided by the associated high-speed synchronous modem or by the DQ11's internal crystal clock option (DQ11-KA).

The DQ11 provides parallel-to-serial and serial-to-parallel data conversion, voltage or current level conversion, character recognition, error detection, and data set control for half- or full- duplex operation. The interface is compatible with the Bell 201, 208, and 303 modems, or their equivalents.

Transmit and receive data transfers between the PDP-11 UNIBUS and the DQ11 are handled as direct memory or device access data transfers without processor supervision. As a direct memory access device, the DQ11 provides extremely fast access to the PDP-11 UNIBUS and can transfer data at exceptionally high rates once it gains control. The PDP-11 processor state is not affected by these types of transfers, since they occur on a cycle-steall basis.

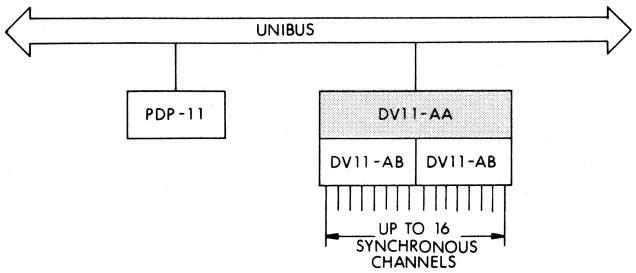
The DQ11 contains diagnostic-controlled, self-testing facilities to ensure both the quality of the data converters and control logic, and to minimize on-line malfunctions.

PDP-11

DV11 Synchronous Multiplexer

JULY 1976

The DV11 is a synchronous multiplexer which permits eight or sixteen synchronous lines to be interfaced to a PDP-11. It is designed to relieve the PDP-11 processor of almost the entire overhead associated with interrupt handling, character processing and CRC/LRC calculations.



FEATURES

Throughput

- Direct memory access data transfers for both reception and transmission
- 8 or 16 line multiplexer
- Total 16 line throughput of up to 38,400 characters per second (9600 baud full duplex for each line)
- 128 character receiver buffer

Flexibility

- Control table scheme provides programming flexibility, particularly for special character and protocol handling.
- Open-ended flexible design–hardware not committed to any specific protocol.
- Modem control.
- Two program-selectable sync characters for each line.

Performance

- Program-selectable block checks (LRC-8, CRC-16, CRC/CCITT) calculated by the hardware.

DESCRIPTION

The DV11 is a high-performance interface for connecting the PDP-11 to multiple synchronous lines (in 8- or 16-line groups). It is designed to relieve the PDP-11 processor of almost the entire overhead associated with interrupt-handling, character-processing and CRC/LRC operations. DMA transfers are performed on transmit and receive. It contains advanced features for special-character and protocol handling.

It provides very high throughput (up to 38,400 characters per second total for all 16 lines) and extremely flexible handling of special data link characters. High throughput is achieved by use of direct memory transfers on both transmission and reception. Flexibility is achieved, without committing hardware to any specific protocol, through the use of control bytes stored in core tables. The program can specify parameters in each control byte, thus providing flexibility for requirements within a specific application.

The DV11 contains provisions for up to eight reception modes for use with character-oriented protocols (for instance, there are modes for transparent data reception and for normal text reception). The action taken in each mode and the transition from one mode to another are controlled by control tables located in core memory. A control table for an individual reception state consists of 256 bytes–one for each of the possible characters that can be received during the reception.*

The DV11 control logic can perform block check calculations for longitudinal redundancy checks (LRC), and cycle redundancy checks (CRC-16 and CRC/CCITT).

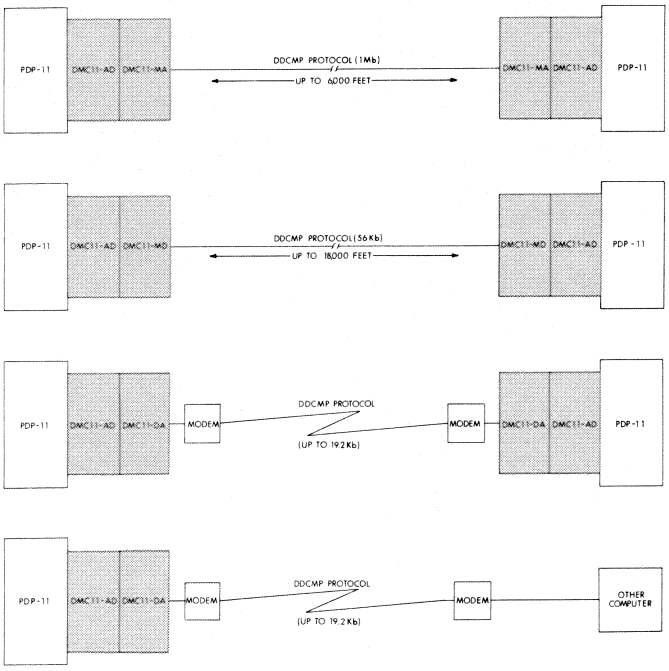
Two sync characters may be manually pre-selected for each four-line group. Then the program can select from either of those two sync characters for each individual line. For transmission, the same sync character is used as the transmitter fill-character or an "all 1's" condition can be sent.

*Typically, control bytes are used to indicate how the character is to be handled, whether an interrupt is to be generated, and whether to include the character in the block check.

PDP-11
DMC 11 Network Link

JULY 1976

The DMC11 Network Link is designed for high-performance interconnection of PDP-11 computers in network applications. Where computers are located in the same facility, DMC11's can be configured for high-speed operation (56,000 or 1,000,000 bps) over inexpensive coaxial cable; the necessary modems are built-in. Where the computers are located remotely and connected via common-carrier facilities, DMC11's can be configured to interface to synchronous modems such as the Bell models 208 and 209, or other modems conforming to the R5232C standard.



FEATURES

Throughput

- DDCMP (Digital Data Communications Protocol) communications protocol implemented by hardware for reliable data transmission, high throughput, low processor overhead and ease of programming.
- Pipelined operation for high throughput by overlapping data transmission, program operation and propagation delays.
- 16-bit direct memory access transfers for minimum interference with processor operation.

Speed

- Local operation at 1,000,000 bits per second (full or half duplex) over coaxial cable up to 6,000 feet long.
- Local operation at 56,000 bits per second (full or half duplex) over coaxial cable up to 18,000-feet long.
- Remote operation over synchronous modems at speeds up to 19,200 bits per second (full or half duplex) using an EIA interface

Power

- Local or remote interconnection of computers over a serial synchronous link.
- When operating in half-duplex only a single cable is needed.
- Private wire or switched network remote operation
- Down-line loading of satellite computer systems
- Ability to initialize an incorrectly functioning satellite computer system by command over the link (remote load detect).
- Communication between DMC11's or between a DMC11 and other synchronous interfaces that can support the DDCMP protocol.

DESCRIPTION

Since the DMC11 contains hard wired DDCMPs, it has a number of advantages over conventional interfaces which require a combination of hardware and software to implement a protocol. Programming is greatly simplified. Programming the DMC11 does not require extensive communications expertise. PDP-11 memory and processor time are not wasted with instructions implementing the protocol. Throughput is enhanced because the DMC11 microprocessor operates at high speed and is not delayed when the processor has to perform high-priority tasks.

The DMC11 ensures reliable data transmission by implementing the DDCMP protocol in hardware using a high-speed microprocessor. The DDCMP protocol detects errors on the channel interconnecting the systems by using a 16-bit Cyclic Redundancy Check (CRC-16). Errors are corrected, when necessary, by automatic retransmissions. Sequence numbers in message headers ensure that messages are delivered in proper order with no omissions or duplications.

Errors are commonplace on cables or other communications channels more than a few feet in length. Reliable data transmission requires a protocol. The DMC11 takes care of the details of protocol operation including character and message synchronization, header and message formatting, error checking and retransmission control. The PDP-11 program need not worry about these details. Where the computers are located in the same facility, DMC11s can be configured for high-speed operation (56,000 or 1,000,000 bits per second) over inexpensive coaxial cable. The necessary modems are built-in. Where the computers are located remotely and connected via common carrier facilities, DMC11s can be configured to interface to synchronous modems such as the Bell Models 208 and 209, or other synchronous modems conforming to the RS232C standard.

Two PDP-11 computers can be connected by a pair of DMC11s. For remote operation, a DMC11 can communicate with a different type of synchronous interface or even a different type of computer, provided that the remote system has implemented the DDCMP (Digital Data Communications Message Protocol) protocol.

PIPE LINING

The DMC11 supports full- or half-duplex operation. Full-duplex operation offers the highest throughput and is used when the communications facilities permit two-way simultaneous operation. Data and/or control messages can be exchanged between the two computer systems simultaneously in both directions. The DDCMP protocol permits continuous simultaneous transmission of data messages in both directions when buffers are available and there are no errors on the channels.

In order to take advantage of this pipeline capability, the DMC11 permits the PDP-11 program to queue as many as seven buffers containing messages for transmission and as many as seven empty buffers for reception. By queuing up multiple buffers, the program can effectively overlap PDP-11 processing with data transmission.

Transmissions do not have to stop while the program responds to an end-of-message interrupt. The DMC11 will interrupt the PDP-11 when a message has been successfully transmitted or received. At this time the program can supply a new buffer to keep the pipeline filled.

DOWN-LINE LOADING AND REMOTE LOAD DETECT

The DMC11 supports down-line loading of computer system software. Down-line loading is used when software is centrally stored (in a host system) and distributed over the network links to other systems (the satellite systems). These satellite systems are often small systems with no peripherals available for program loading. Sometimes the satellite systems have disks, but down-line loading is desired to maintain central control over software.